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RESEARCH ARTICLE

DESIGN AND DEVELOPMENT OF C-V METER

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ABSTRACT

The present paper discusses design and development of C-V meter which could be interfaced to PC through microcontroller based smart DAC (Data acquisition card). The C-V meter for the measurement of Capacitance between 2pF to 20nF is designed. The circuit also allows measurement of Quality Factor between 10^1 to 10^4. The circuit designed here is based on Auto balancing bridge technique. A DC bias voltage of $\pm$ 10 V is selected in the present case. The results on simulation using MULTISIM 11.0 (version 11.0.1) are also elaborated in the present paper.

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INTRODUCTION

One of the primary instruments for the characterization of ferroelectric/dielectric materials is its characterization for electric tunability (Zimmermann *et al*., 2004).

The electrical tunability is defined as given below

$$\tau = \frac{\varepsilon(E) - \varepsilon(0)}{\varepsilon(0)} \quad (1)$$

Where, ε (E) and ε (0) are the value of dielectric constant with and without applied electric Field E. The dielectric constant is measured by the determination of capacitance formed using given dielectric material. Usually, the present day applications require thin film of ferroelectric/dielectric compounds having a useful magnitude of electric tunability (τ). Such system could be used in formation of tunable filters, resonators etc. for both RF as well as Micro-wave frequency range (Jain *et al*., 2003).

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Thus the basic requirements of the measurement of the tunability is the measurement of capacitance at certain frequency of ac excitation superimposed with a $\pm$ DC bias voltage. There are few commercially available Test and Measurement instruments (T&M), which posses the option of C-V measurement from 1 to 10 MHz, for example Agilent LCR-Q Meter 4279A, 4980A, 4294A, HP 4284, Wainekerr 6500B. It is observed that these commercially available T&M instruments are not cost–effective and need large capital investment, nearly 8 to 10 Lac Rupees. The present paper is an attempt towards design and development of exclusive C-V meter operating at few selected frequencies (viz. 100 KHz, 500 KHz and 1 MHz). Further development of this product is expected to provide a detailed understanding for circuit design and development of variable frequency LCR meter and correct estimation of error analysis will be readily available. Therefore the present paper reports, details of the activity of design of C-V meter. Here the various available schemes of C-V meter instruments are compared and a new scheme is proposed. The new scheme is expected to have minimum possible error in respect of amplitude as well as phase measurement.

The literature survey shows that there are three basic methods of measurement of the capacitance.

- Classical ac impedance measurement
- Quasi-static capacitance measurement
- RF Technology capacitance measurement

Out of these the quasi-static method provides a dc value of capacitance, while the other two methods are meant for higher frequencies of ac excitation (www.keithley.com). But present day instruments are observed to employ either Auto balancing bridge method (Classical ac Impedance measurement) or RF Technology for measurement of capacitance and corresponding Q. Out of the above methods the Auto balancing bridge method has maximum advantages over other methods. Here the reported advantages of this method are (www.agilent.com/ find/impedance):

- Wide frequency range 20Hz to 110 MHz
- High accuracy over wide impedance measuring range
- Grounded device measurement

Another advantage of this method is easier way of addition of DC bias voltage to the ac excitation voltage. Usually Operational amplifier adder circuit could be adopted for this purpose. Therefore no additional phase error, due to coupling transformer will be involved in this scheme of measurement of C-V. The only limitation of the scheme will be a restriction on the magnitude of DC bias voltage, because of the rated output voltage of the operational amplifier used. A large amount of reference material is already available, for the Auto balancing bridge method discussed in paragraph above. But the detailed comparative account is provided by M/s. Agilent Technology only (Scott).

Basic Concept

Considering the virtues of auto-balancing bridge technique and easier adoption of the scheme for addition of the bias voltage, it is proposed to adopt this scheme for the development of C-V meter. The basic scheme of measurement of capacitance (i.e. Auto balancing bridge method) of Device Under Test (DUT), Cx is usually represented as a parallel combination of R_P and C_P since its value is small. Here the impedance (Zx) of Cx could be expressed as

$$Z_X = Z'_X - jZ''_X = \frac{R_P}{1+\omega^2 C_P^2 R_P^2} - j\frac{\omega C_P R_P^2}{1+\omega^2 C_P^2 R_P^2} \quad (2)$$

Where Z'_X is real component of Z_X,

while Z''_X is imaginary component of Z_X.

Equation (3) gives Quality factor,

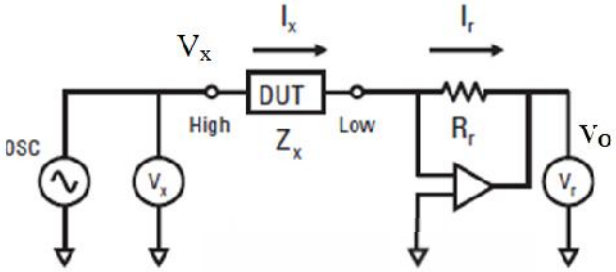
$$Q = \frac{Z''_X}{Z'_X} = \omega C_P R_P \quad (3)$$

Equation (4) gives admittance of C_x which is represented as Y_x,

$$Y_X = G_P + jB_C = {}^1/_{R_P} + j\omega C_P \quad (4)$$

Where G_P is a parallel conductance and B_C is susceptance of capacitor (Scott).

Figure (1) shows Auto balancing bridge method for measurement of capacitance.



$$V_X/Z_X = I_X = I_r = V_r/R_r$$

$$\therefore \quad Z_X = V_X/I_X = R_r * V_X/V_O$$

Now the current through DUT is I_x as shown in Fig. 1, which is equal to $Y_x * V_x$, by keeping V_x constant and knowing the I_x, we may determine required value of C_p and Q, assuming that ω is known and constant.

Usually I_x is subjected to I to V conversion and corresponding output voltage referred as V_o. Thus in-phase component of the division V_o/V_x is proportional to $1/R_p$, while a component π/2 out of phase corresponds to ωC_P. The further numerical processes to determine the other impedance parameters such as quality factor (Q), loss tangent (tan δ) and impedance Z (i.e Z = Z′ + jZ″), will be processed by PC interfaced to the circuit, where the PC interface is a microcontroller based DAC. Usually the microcontroller based DAC is smart enough to make the CV meter, a programmable unit. Also the DAC can be controlled through the virtual instrumentation system (LABView).

Circuit Description

Figure (2) shows signal generator block, including Sine wave generator (Wien Bridge oscillator circuit) capable of producing sine wave of 100 KHz, 500 KHz, 1 MHz and a sine to cosine converter (Integrator circuit). An attenuator to limit the output of sine wave for 50 mV and output buffer is a part of this block. Further, TTL level reference voltage in phase with sine wave and cosine wave are also produced in this block of signal generator. Therefore the same circuit may also work for a standalone C-V meter.

Further a programmable staircase shape triangular wave is generated as the part of this block. Here the amplitude of the triangular wave and number of steps per cycle are programmable. Usually this type of oscillator could be devised using micro-controller based circuit or a PC add-on card. At present a low-frequency triangular wave generated using an operational amplifier is utilized as variable DC bias (± 10V) for testing the designed C-V meter. The auto balancing bridge method is utilized here for impedance measurement. Fig. 3 shows block diagram of the actual measurement circuit. The circuit comprises of addition of ac excitation and DC bias voltage.

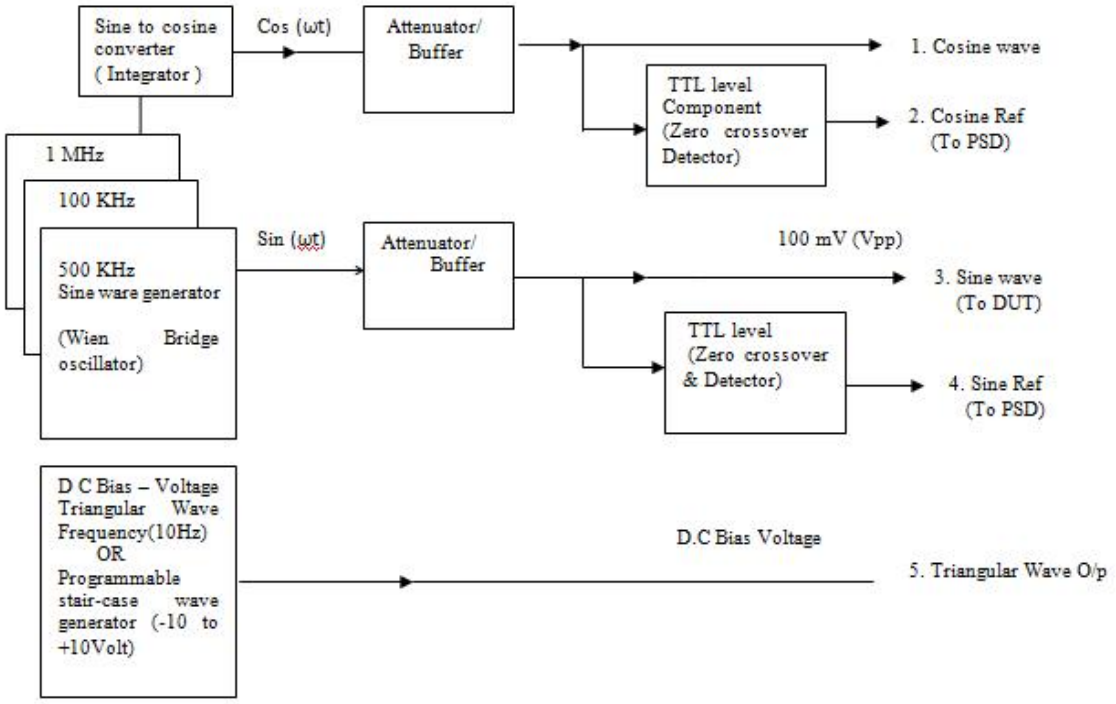


Fig. 2. Signal Generator Block Diagram

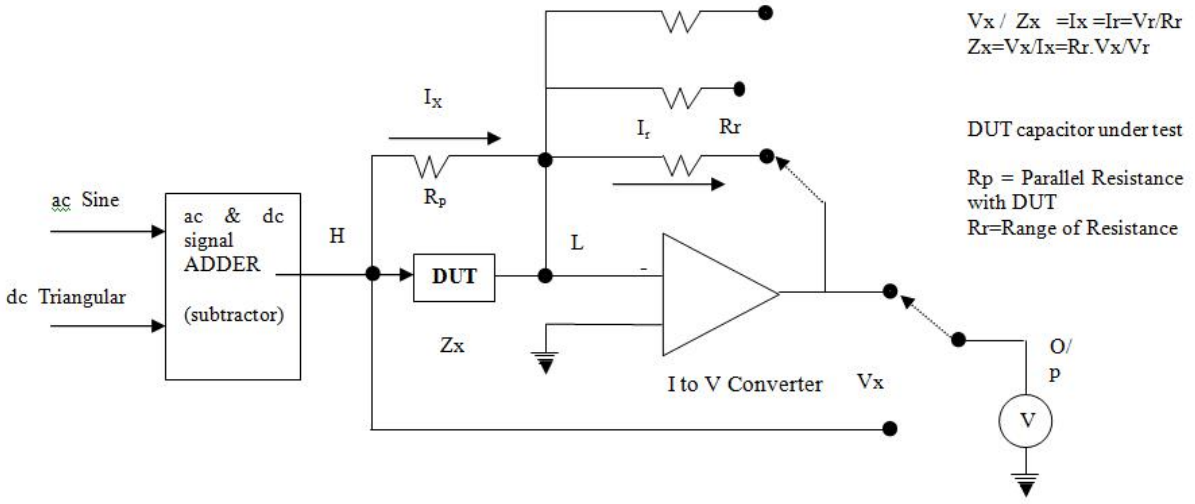


Fig. 3. Auto Balancing Bridge Method (Parallel Equivalent Circuit Mode)

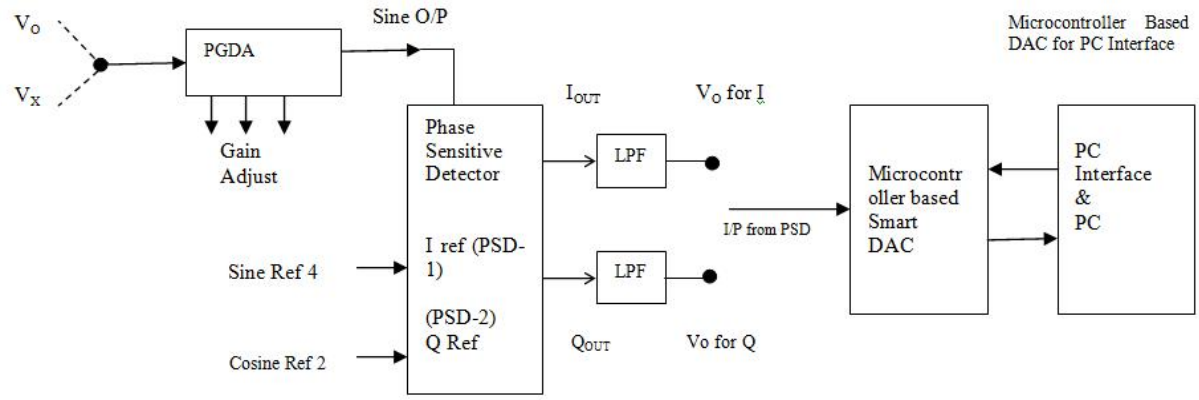


Fig. 4. Phase Sensitive Detector

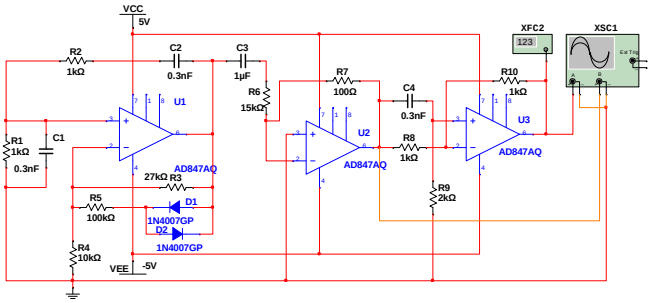


Fig. 5a Wien Bridge Oscillator, Attenuator, Integrator

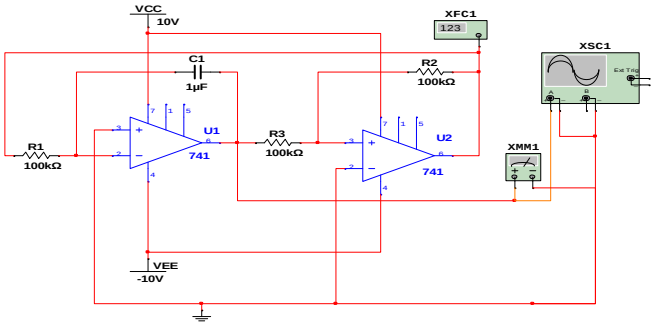


Fig. 5b Triangular Wave Generator for dc Excitation

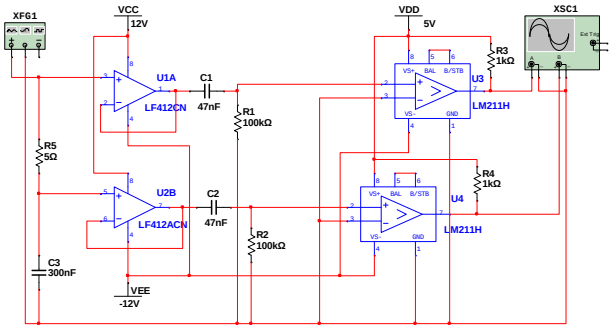


Fig. 5c. Sine and Cosine Reference TTL

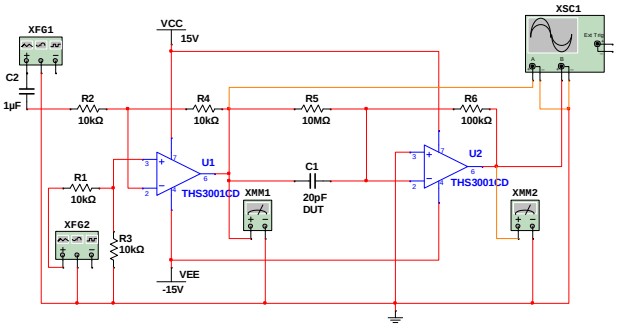


Fig. 5d. Capacitance Voltage Measurement Circuit

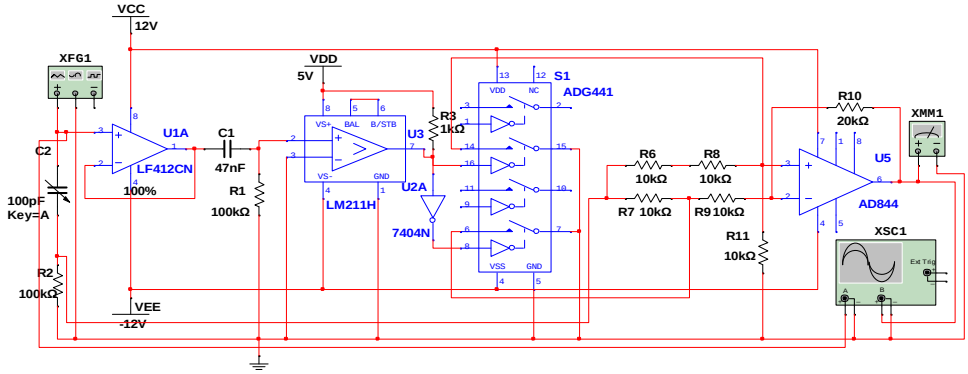


Fig. 5e. Phase Sensitive Detector (Sine Reference)

Table 1. Measurement of simulated output voltage for above designed C-V meter

Used Combinations			Theoretical Values (mV)	Simulated O/P Values (mV)
DUT	R_P Ohm	R_r Ohm		
20 pF	10M	100K	233.37	204.123
20 pF	1M	100K	226.56	204.121
10 pF	10M	100K	111.68	102.029
2 pF	10M	100K	22.33	20.405
200pF	10M	10K	233.37	221.295

In actual practice operational amplifier subtractor circuit is designed to achieve the addition of ac and dc signals.

The output of above circuit is applied to the DUT, the current I_x flowing through DUT and voltage across DUT as V_x are interfaced to sine and cosine wave phase sensitive detector circuits.

The operational amplifier I to V converter having range resistor R_r converts the current I_x into output voltage to V_O. The vector voltage V_x and vector voltage V_O are divided together and interfaced to the phase sensitive detector circuits (PSDs). Hence $1/R_P$ and ωC_p could be determined by calibrating the output voltages of the sine phase and cosine phase PSD respectively.

Fig. 4 shows phase sensitive detector circuit. To measure phase and magnitude of V_o / V_x, two separate phase sensitive detector circuits with sine and cosine reference voltages (TTL level) are used in present case. Usually the V_x is set a specific value of $1x10^{-1}$, $1x10^{-2}$, $1x10^{-3}$ (Ithaco Application Note IAN-47). At present, we are using V_x = 50 mV (i.e. 0.5 x 10^{-3}V). The outputs of PSDs could be connected to the DVM, after proper scaling (PGDA), to get stand-alone CV Meter. Also the outputs of PSDs could be connected to the Microcontroller based smart DAC, which may be interfaced to PC for the further numerical processes and analysis to determine various related parameters

Fig. 5 shows the actual circuits designed in the present case.

- Wine bridge Oscillator, Attenuator, Integrator
- Triangular Wave Generator for dc Excitation
- Sine Cosine references (TTL Pulse)
- Capacitance Voltage Measurement Circuit (Auto Balancing Bridge)
- Phase sensitive detector circuits (Sine Reference)

The Test Procedure and Result

The simulation software (MULTISIM 11.0), is used to test the following circuits.

- Sin wave generator (wine bridge oscillator circuit) for 500 KHz (50 mV p-p) as an ac excitation frequency, Attenuator, Sin to cosine converter (Integrator)
- Low-frequency (50Hz / $\pm$10V) triangular wave generator as dc excitation
- Buffer, TTL pulse generator using Zero crossing Detector as a Sine and Cosine reference
- Capacitance Voltage Measurement circuit (Auto Balancing Bridge)
- Phase sensitive detector circuit (Sine Ref.)

It is observed that the magnitude of the outputs of simulated circuit do not show any measurable error between sine wave and TTL level Sine reference. Also output amplitude and phase of different simulated circuits do not have any significant difference as compared to the corresponding predicted theoretical values (i.e. the errors are within the predicted limit).

Measurement of simulated output voltage for above designed C-V meter. Frequency utilized 500 KHz (50 mVp-p), ac Input Voltage. At present, five different configurations of DUT are selected and tested as sample cases; the Table I shows the comparative account for theoretical results and actual simulated outputs to these combinations. From the TABLE- I it could be said that the accuracy of the circuit is greater than ± 95 %.

Conclusion

The present attempt is successful effort of the C-V meter design. Further the actual test circuits are being developed for the design and test of a prototype.

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