*Available online at http://www.journalcra.com*

*International Journal of Current Research*
*Vol. 9, Issue, 03, pp.47320-47329, March, 2017*

**INTERNATIONAL JOURNAL OF CURRENT RESEARCH**

**ISSN: 0975-833X**

## RESEARCH ARTICLE

# LEAKAGE CURRENT AND POWER REDUCTION TECHNIQUES IN COMBINATIONAL CIRCUITS

***Dr. Sunil Jacob and Vinny Wilson**

Department of Electronics and Communication, SCMS School of Engineering and Technology, MG University, Ernakulam-683582, Kerala, India

**ARTICLE INFO**

***Article History:***
Received 12th December, 2016
Received in revised form
27th January, 2017
Accepted 25th February, 2017
Published online 31st March, 2017

***Key words:***
Conventional logic, Static and dynamic power, GDI logic, Leakage current reduction methods, Power reduction and consumption, Transistor count, Sleep transistor.

**ABSTRACT**

Power consumption and it's reduction is one of the primary concerns in today's VLSI design because of two main reasons, one is the long operating life requirement of phone battery and portable devices and second is due to increasing number of transistors on a single chip which leads to high power dissipation and it can lead to reliability and IC packaging problems. Power reduction has become an important issue in digital circuit design, especially for high performance portable devices (such as cell phones, PDAs, etc.). Thus, it is evident that methodologies for the design of high-throughput, low-power digital systems are needed. A chip's maximum power consumption depends on its technology as well as its implementation. Due to scaling down of technology and when CMOS circuits are powered by lower supply voltages, standby leakage current becomes significant. Also threshold voltage is reduced due to scaling which leads to the increase in sub- threshold leakage current and hence there will be increase in static power dissipation. In order to reduce the static power dissipation, one has to give up the circuit performance and area of the given circuit. This project discuss about various leakage current reduction methods that will be useful for both Conventional and Gate diffusion input (GDI) logics inorder to reduce the static power, dynamic power and also consider the area by using minimum number of transistors. These all were done in 95nm technology using Tanner EDA V13.0 Tool.



**Citation: Dr. Sunil Jacob and Vinny Wilson**, **2017.** "Leakage current and power reduction techniques in combinational circuits", *International Journal of Current Research*, 9, (03), 47320-47329.

## INTRODUCTION

Need for low power VLSI chips arise from evolution forces of integrated chips. VLSI design is an emerging technology which was introduced by Carver Mead and Lynn Conway for saving the area of chips by minimizing the interconnect fabric area. Low power should be achieved precisely because of desirability of portable devices like cell phones, batteries and in biomedical fields (e.g.: heart pacemakers), however when power dissipation increases it requires larger heat sinks hence there will be increase in the area. So a new solution is to be provided for low power applications for the designers in VLSI circuit design process. Especially, this work focuses on the reduction of leakage current and power, which is showing an ever-increasing growth with the scaling down of the technologies. In *electronics*, leakage refers to an abrupt energy loss from a charged *capacitor*. Initially this was caused by the electronic devices that is attached to the capacitors, such as transistors or diodes, which conduct an insignificant amount of current even when they are turned off. Even though this off current is smaller than the current that flows through the device when it is on, but still the current will slowly discharges through the capacitor. Another major source to leakage is from the undesired imperfections of some dielectric materials used in capacitors and is known as dielectric leakage. Power optimization means the use of *electronic design automation* tools to optimize (reduce) the power consumption of a digital design, such as that of an *integrated circuit*, by preserving the functionality the functionality of the circuits. The growing market of portable devices such as mobile phones, gaming equipment, etc. & electronic systems with batteries demands the micro-electronic circuit's designers to implement ultra-low power circuits. As the integration, size, and complexity of the chips increase drastically, the difficulty in providing adequate cooling might either increase the cost or limit the performance or functionality of the computing systems which make use of the integrated circuits. As the technology scales down to 65nm, dynamic power dissipation will not increase significantly. However, the static or leakage power tends to be the same or will try to exceed the dynamic power beyond 65nm technology. Hence the techniques to reduce power dissipation are not limited to dynamic power. This project discuss about the circuit and logic design approaches to minimize Dynamic and Leakage power dissipation. Power optimization in a processor can be achieved at various abstract levels. So there should be optimization at Circuit and Technology levels which is also very important for miniaturization of ICs.

Total dissipated power in a CMOS circuit is the sum total of dynamic power, short circuit power and static or leakage power. Low-power designs imply the ability to reduce all the three components of power consumption in CMOS circuits during the manufacture of low power electronic products. Power consumption is now the major technical problem facing the semiconductor industry. As leakage current becomes the major source of power consumption, the industry must re-evaluate the power equation that degrades the system performance, chip size, and cost. So we have to reduce the power & leakage currents in both combinational sequential circuits. In recent years, low power circuit design has been an important issue in VLSI design areas. This work is about the Leakage current & Power reduction in CMOS technology using two different topologies such as Static or Conventional CMOS and Gate Diffusion Input (GDI) logic.

**Corresponding author*: **Dr. Sunil Jacob and Vinny Wilson**
Department of Electronics and Communication, SCMS School of Engineering and Technology, MG University, Ernakulam-683582, Kerala, India.

# LITERATURE REVIEW

**Sources of Power Dissipation in VLSI Circuits**

Power dissipation has become primary factor in VLSI design. The total power is given by:

a) Dynamic switching power
b) Static power (leakage power)
c) Short -circuit power

Total power (P) = $P_{switching} + P_{leakage}$

Total Power (P) = $\alpha\, C_L Vdd^2\, f \; + \; I_{leakage}\, Vdd$

**1. Dynamic power**

Dynamic power dissipation occurs when the circuit is operational, i.e. the circuit is performing some task on some data.

**a) Charging and discharging of load capacitances**

Charging the various load capacitance sin CMOS circuits causes power dissipation (mostly gate and wire capacitance) whenever they are switched ON. In one cycle of CMOS logic, current flows from $V_{DD}$ (supply voltage) to the load capacitance to charge it and then at the time of discharging it flows from the charged load capacitance ($C_L$) to ground. Therefore, in one cycle, a total charge, $Q=C_L V_{DD}$ is thus transferred from $V_{DD}$ to ground. Then the switching frequency is multiplied with the load capacitance to get the current used, and then again multiply it with the average voltage to get the switching power dissipated by a CMOS device. When the gates of transistors do not operate/switch at every clock cycle, they are often followed by a factor α, called as the activity factor. Now, the dynamic power dissipation can be denoted as,

$$P_{switching} = \alpha\, C_L Vdd^2\, f$$

If the clock rises and falls at every complete cycle, the system will have an activity factor α=1. Most of the VLSI circuits has an activity factor of 0.1.When load capacitance values were corrected and estimated properly on a node along with its activity factor, the circuit designers can calculate the dynamic power dissipation at that node efficiently.

**b) Short-circuit power dissipation**

During the time of transition there is a finite rise/fall time for both PMOS and NMOS. For example, from off to on time, both the transistors will be on for a small period of time and current will find a path directly from $V_{DD}$ to ground, hence creating a short-circuit current. Thus Short-circuit power dissipation increases with rise and fall time of the transistors. During 1990s, as wires on chip became narrower and the long wires became more resistive, an additional form of power consumption became more significant. Thus CMOS gates at the end of those resistive wires shows slow input transitions. Both the NMOS and PMOS logic networks were partially conductive and current flows directly from $V_{DD}$ to $V_{SS}$ (ground), during the mid-period, when there are changes from one state to another. This power is called as crowbar power. Only careful designs helps the designers to avoid the weakly driven long skinny wires and in turn ameliorates this effect, but crowbar power will be always a substantial part of dynamic CMOS power.

$$P_{short-circuit} = t_{sc} I_{peak}\, Vdd$$

**2. Static power**

Static power dissipation will be an important issue when the circuit is not functioning or in a power-down or inactive mode. The gate–source threshold voltage of both NMOS and PMOS transistors will be low and thus the *sub-threshold* current through the device changes rapidly or will drop exponentially. To increase the speed of designs, manufacturers have switched to the constructions that have lower voltage thresholds. Designs (e.g. desktop processors) which include tremendous number of circuits which are not actively take part in the switching and still consumes power because of the presence of leakage current. Such designs consume leakage power which is the significant portion of the total power dissipation.

$P_{leakage} = I_{leakage}\, Vdd$

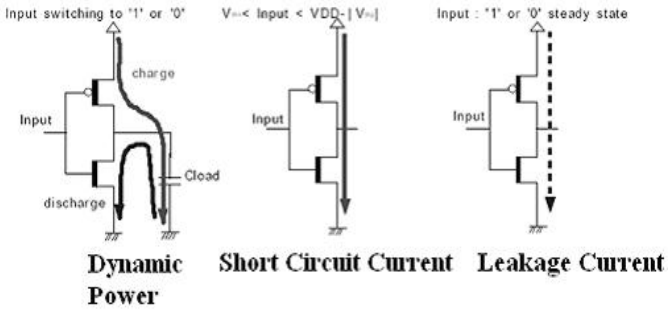


**Fig.1. Components of Power in CMOS circuit**

**Table 1. Comparison table for leakage current reduction techniques (Wang and Calhoun, 2006; Srikanth Katruea and Dhireesha Kudithipudi, 2008; Mutoh *et al*., 1995; Varsha Bendre and Kureshi, 2015)**

| Techniques | Advantages | Disadvantages |
|---|---|---|
| Sleep transistor | simple circuitry | generates noise in circuits |
| Sleepy stack | single threshold transistors, less delay compared to force stacking approach | sleep transistors need control circuit, area increases, less power savings |
| Sleepy keeper | less area is required | decreases the performance |
| Power gating With stacking | More leakage savings in both operating modes | Delay increases, Area increases, Complex to fabricate |
| Power gating With PMOS And NMOS Sleep Transistor | Large power savings, most preferred method | Control circuit is needed. |
| Lector | Control circuit is not required, Best power savings in both the modes of operation | Delay increases, Sizing Sleep transistors. |
| Forced Stacking | Easy to implement, Leakage savings, Easy to fabricate | Propagation delay Increases |
| Zigzag | Reduces wake up overhead of sleep transistors | Requires additional circuitry to generate specific input vector |
| SCCMOS with PMOS and NMOS sleep Transistor | Best power savings, Easy to Fabricate | Control circuit is needed |
| GALEOR | Reduces Voltage Swing | Propagation Delay Increases |
| Sleepy pass gate technique | Increases resistance & thereby reduces leakage power | Delay increases |
| VCLEARIT | Operates As Conventional Logic | Delay Higher Than Sleepy Pass Gate technique |

**Leakage Current Reduction Methods**

There were several methods that can be used in static or conventional logic inorder to reduce the leakage current, which occurs when the circuit is not switching or in OFF state. This project focuses on many leakage reduction methods and were using only some methods in the

proposed design. From the selected few leakage methods the best method selected. In sleep transistor approach authors Kawaguchi, Dhananjay & *et al*. (2000, 2010) say that additional sleep transistors are introduced into the network. They also said that other technique to reduce leakage current is by stacking (Kawaguchi *et al*., 2000; Dhananjay *et al*., 2010; Smita Singhal *et al*., 2015) of the transistor. In Sleepy Keeper approach authors Kawaguchi, Smita Singhal & *et al*. (2010, 2015) say that additional NMOS is aligned collaterally to the pull-up sleep transistor which connects $V_{DD}$ to pull-up network and an additional PMOS is placed equidistant to the pull-down sleep transistor which connects pull-down Network to the Ground. So the state is saved in sleep mode. In normal stacking technique authors Abdollahi, Smita Singhal, P. S. Aswale & *et al* (2004, 2015 & 2013) say that an additional transistor is introduced for every input of gate in both P and N networks. The next method is dual stack approach which was introduced by the author C. Jagadeesh and *et al*. (2013). In sleep mode, the sleep transistors are off. Similarly we can do dual triple stack approach (2013) by having triple pmos stack at the footer/bottom of the circuit. Abdollahi, Smita Singhal & *et al*. (2004, 2015) say that MTCMOS is a technique used to design CMOS circuits with high, low and normal voltage transistors. Using this technique, selective scaling of threshold voltage can be done along with supply voltage thus will be able to increase the circuit speed without increasing the sub threshold leakage currents. In DTMOS method (Abdollahi *et al*., 2004; Smita Singhal *et al*., 2015) they also said that, the body and the gate of each transistor are tied together such that when the device is off, the leakage is low. The other method introduced by them inorder to modify the threshold voltage of a transistor is known as variable threshold CMOS technique (Abdollahi *et al*., 2004; Smita Singhal *et al*., 2015) (VTCMOS).

In this technique during standby mode, threshold voltage (Vth) is elevated to a higher value by making substrate voltage either higher than supply voltage (for PMOS) or lower than ground (for NMOS). Pusha Saini & Rajesh Mehra (2012) said that in LECTOR method two leakage control Transistors (LCTs) were introduced to each of the CMOS gates. This is done by adding a PMOS transistor to the Pull up network and a NMOS transistor to the pull down network. The gate terminal of one the LCT is regulated by the source terminal of the other and any one of the LCTs will be in OFF state for any input given to the CMOS gate, by this an extra resistance will be formed in between the path (from supply to ground). This decreases the sub-threshold leakage current and there by the static power is reduced. These authors again said that Zigzag method (Pushpa Saini and Rajesh Mehra, 2012) reduces wakeup overhead of propagation delay caused by the sleep transistors.

This is done by placing the alternating sleep transistors either on pull-up or pull- down networks and will be off for a given specific input vector. In Zigzag keeper approach, it can be noticed that sleep transistor is added in base approach according to given logic value. Kaushal Kumar Nigam, Malviya and *et al*. (2013, 2012) say that it may be logic 0 or 1 value at the input of base approach. It can be seen that as Vsb1 increases leakage current decreases. The body effect and Vth also increases due to which performance gets degrade (Aswale and Chopade, 2013). P. S. Aswale and *et al*. said that variable body biasing technique (Aswale and Chopade, 2013) uses two parallel sleep transistors in pull up network and two parallel sleep transistors in pull down network. Kawagudi, Smita Singhal & *et al*. (2000 & 2015) said that SCCMOS scheme is proposed to achieve high-speed and low stand-by current. By overdriving or under driving the gate of a cut-off MOSFET, the SCCMOS prevent the leakage current in stand-by mode while high speed operation in an active mode is possible with low threshold voltage. Smita Singhal & *et al*. (2015) says that VCLEARIT technique (VLSI CMOS Leakage Reduction Technique) is the combination of one high $V_t$ (threshold voltage) sleep transistor and two standard $V_t$ sleep transistors. In the circuit, sleep signal is '0' during active mode and '1' during standby mode. During active mode, P1 is on P0 and N0 are off. Thus the circuit operates as a conventional design. Srikanth Katrnea, Smita Singhal & et al. (2008, 2015) says that GALEOR technique introduces the Gated Leakage Transistors in the CMOS design. Due to the Gated Leakage transistors, there is a threshold voltage loss which reduces the voltage swing of the circuit. The propagation delay of the circuit is also increased. In dual sleep method Smita Singhal & *et al*. (2015) says that two sleep transistors in each NMOS or PMOS block are used. Dual sleep approach uses the advantage of using the two extra pull-up and pull- down transistors in sleep mode either in OFF state or in ON state. Since Dual Sleep portion is common in the circuitry therefore less number of transistors is required. These authors again say that Sleepy Pass Gate Technique (2015) increases the resistance of the path from supply voltage to ground in the standby mode thereby reducing the leakage power. Malviya and *et al*. (2013) says that leakage feedback approach is based on the sleep approach. However, the leakage feedback approach uses two extra transistors in order to maintain the logic state during sleep mode, and the two transistors are driven by the inverter output which is driven again by the output of the circuit utilizing leakage feedback. Archana Nagda and *et al*. (2012) proposed a circuit family known as drain gating techniques, which is capable of maintaining the original signal quality and avoiding some problems related with leakage reduction. This reduces the leakage current by adding extra sleep transistors between the PMOS pull-up and NMOS pull-down networks. There are three combinations for drain gating: Power Gating, Drain-Header & Power-Footer Gating (DHPF) and Drain-Footer & Power-Header Gating (DFPH). It also includes sleep transistor technique. Aswale and *et al*., introduce a new technique called dual threshold transistor stacking (2013) which is a hybrid version of stack and MTCMOS. It takes the advantage of both techniques i.e., sleep transistors are modified or reconstructed with stack effect. Smita Singhal & *et al*. (2015) have again introduced the combined MTCMOS and transistor stacking techniques as well as SCCMOS and transistor stacking techniques to form four new techniques. They are hybrid MTCMOS complete stack technique, hybrid MTCMOS partial stack technique, hybrid super cutoff with complete stack technique and hybrid super cutoff with partial stack technique, for the reduction of sub threshold leakage power dissipation in standby modes.

**Low Power Techniques**

In order to reduce the dynamic power of the circuit, this project focused on mainly five factors. They are:

1. Supply voltage scaling (Kim *et al*., 2002; Park and Mooney, 2006)
2. Reducing effecting capacitances (Kim *et al*., 2002; Park and Mooney, 2006)
3. Effects of circuit style (Kim *et al*., 2002; Park and Mooney, 2006; Dhananjay *et al*., 2010)
4. Transistor sizing (Kim *et al*., 2002; Park and Mooney, 2006; Pushpa Saini and Rajesh Mehra, 2012)
5. Switching activity reduction (Kim *et al*., 2002; Park and Mooney, 2006)

But by reducing the supply voltage there will be increase in the delay of the circuit.

**Conventional Logic**

The CMOS logic circuits are categorized into two categories: - static (conventional) and dynamic logic circuits. These two logic styles can be used according to the design requirements such as power consumption, speed and area. In a static logic circuit, we can retain the logic value by using the circuit states while in a dynamic logic circuit a logic value is stored in the form of charge. So, in static logic circuit each output was according to the Boolean function and is taken from drains of both pull- down (NMOS) and pull- up (PMOS) networks. So, at every point the output will be connected to either $V_{DD}$ or GND via a low resistance path. The static logic eliminates pre-charging and decreases extra power dissipation, thus, are used in low power VLSI circuits. Static logic is further of two types:- single rail and dual rail logic. Single rail uses its input either 1 (true) or 0 (complementary) output signals. However dual rail uses its input either true or false and yield both true and false signals as their output

at the same time. Most commonly used static logics are Pseudo-nMOS, static CMOS, transmission gate logic (TGL), pass transistor logic (PTL), Gate diffusion input logic (GDI), pass- transistor logic which is complementary (CPL), and double pass transistor logic (DPL). Static logic uses same number of NMOS and PMOS transistors and always gets the complementary output. For example XOR gate that is constructed using this logic is shown below.

**Table 2. Truth table of XOR gate**

| A | B | XOR=A'B+AB' |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

A full adder is a combinational circuit that performs the arithmetic sum of three input bits: augends Ai, addend Bi and carry input $C_{in}$ from the previous adder. Its results contain the sum, $S_{out}$ and the carry out, $C_{out}$t, to the next stage.

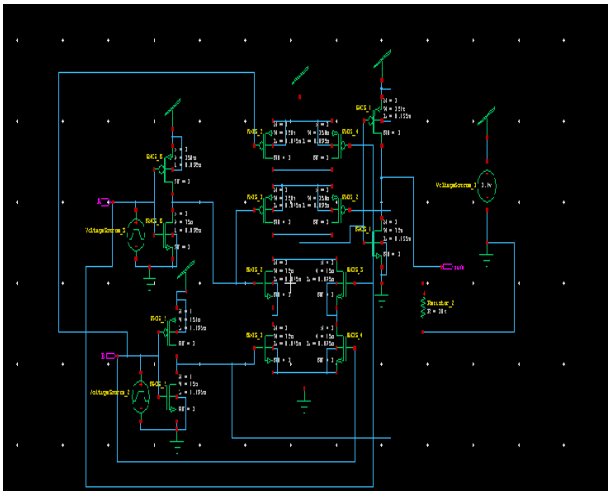

**Fig.2. XOR gate using Static logic**

**Table 3. Truth table for full adder**

| A | B | $C_{in}$ | $S_{out}$ | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Sum = ABC + (A+ B + C) Carry bar
Carry = AB + BC + CA
Carry= AB+C (A+B)

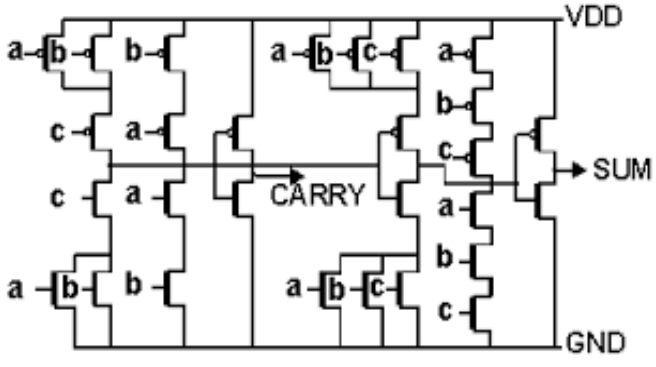


**Fig.3. 28T full adder using Static logic**

This adder cell uses 28 transistor based on regular CMOS structure (pull-up and pull-down networks). Complementary transistor pairs make the circuit layout straight forward. The advantage of using CCMOS is that it has layout regularity, high noise margins and stability at low voltage due to complementary transistor pair and smaller number of interconnecting wires and disadvantage is that it uses $C_{out}$ signal to generate sum which produces an unwanted additional delay. It has weak output driving capability due to series transistors in output stage and consumes more power and large silicon area. $C_{out}$ is generated first using above $C_{out}$ equation. Then the sum is derived from the sum equation shown in above.

**Gate Diffusion Input Logic**

Gate Diffusion Input (GDI CELL) (Vinny Wilson, 2017) is based on the use of a simple cell as shown in figure below. At first glance the basic cell resembles as that of the standard CMOS inverter but there are some important differences:

1. Gate Diffusion Input logic contains three inputs: G (gate input which is common to both NMOS and PMOS), P (is the input applied to the source/drain of PMOS), and N (is the input given to the source/drain of NMOS).
2. Bulks of both NMOS and PMOS are connected to N or P respectively.

The major distinction between the CMOS and GDI based logic design is that the source of the PMOS in a GDI cell (Vinny Wilson, 2017) not uses the supply voltage and the source of the NMOS is not at all connected to the ground. This feature gives an advantage that GDI cell did not want to use ground and supply voltage instead this logic uses two extra input pins which makes the GDI design more flexible than CMOS design. The basic GDI cell shown in Figure was proposed by Morgenshtein. It is a new technique for ultra-low power VLSI circuit design. This logic helps in the reduction of area, power consumption and propagation delay of the VLSI circuits by preserving low complexity of the logic design.

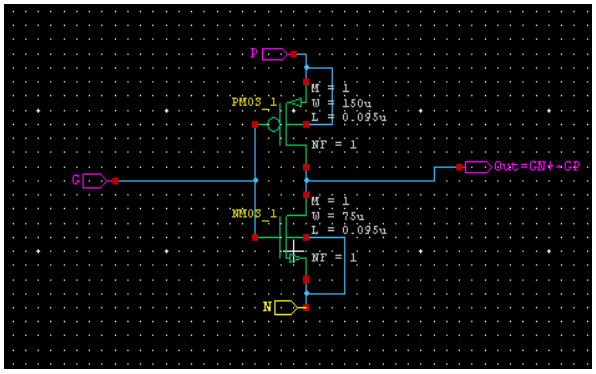


**Fig.4. Basic GDI cell**

Table below shows, how a simple change of the input configuration of the simple GDI cell (Vinny Wilson, 2017) corresponds to very different Boolean functions. Most of the Boolean functions in CMOS technology (contains 6-12 transistors) are complicated ones, and in GDI method implementations, design is very simple (only 2 transistors per function). A simple change of the input configuration of simple Gate Diffusion Input (GDI) CELL is shown in table corresponds to six different Boolean functions. Output of the GDI cell is given GN+~GP.

**Table 4. Some logic functions that can be implemented using a single GDI cell**

| N | P | G | D | Function |
|---|---|---|---|---|
| 0 | B | A | A'B | F1 |
| B | 0 | A | AB | AND |
| 1 | B | A | A+B | OR |
| B | 1 | A | A'+B | F2 |
| 0 | 1 | A | A' | NOT |
| C | B | A | A'B+AC | MUX |
| B' | B | A | AB'+A'B | XOR |
| B | B' | A | AB+A'B' | XNOR |

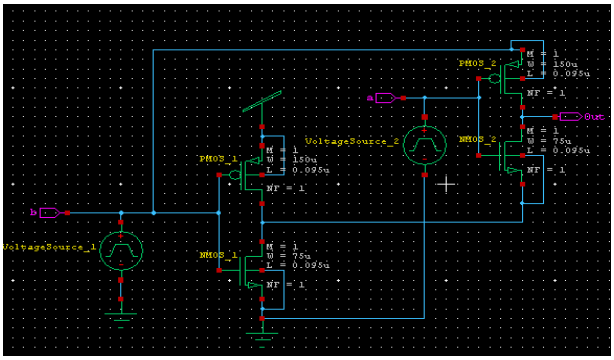

Fig.5. XOR cell with GDI technique

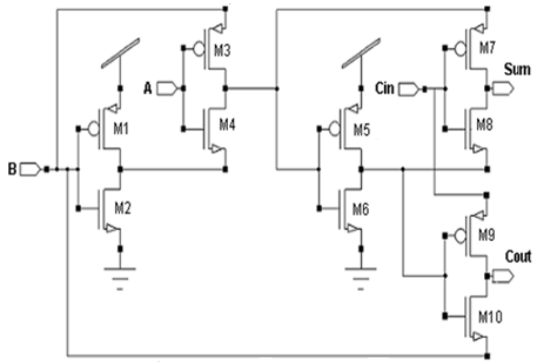


Fig.6. 10T full adder using GDI technique

10T GDI full adder (Vinny Wilson, 2017) consists of three inputs (A, B and $C_{in}$) and two outputs (sum and carry).

Sum, $S_{out}$ = A xor B xor C
Carry, $C_{out}$ = AB+AC+BC

## PROPOSED DESIGNS

Gate diffusion input (GDI)-a new approach of low-power digital combinational circuit design was proposed for static circuits. This technique reduces power consumption, propagation delay and area of digital combinational circuits while it maintains low complexity of logic design. Gate Diffusion Input (GDI) technique represents Boolean functions by minimum number of transistors, so the area will be reduced. Also static logic was implemented using leakage current reduction techniques also by reducing supply voltage and with proper sizing of transistors. This same approach was implemented in GDI logic and compared the leakage, power, and transistor count of both logics.

### A) Proposed method 1

This method implies the improved structure of MTCMOS technique. In this structure, the NMOS high threshold voltage sleep transistor is placed like a stack of two transistors with width twice that of original one. A state is far less leaky with more than one OFF transistor when we compared it to a state where there is only one OFF transistor in the path. This modified method helps in limiting the leakage power to a great extent compared to that of the existing one.

### B) Proposed method 2

It is an improvised structure of existing dual-$V_{TH}$ technique. An NMOS transistor is kept between ground and logic circuit.

In active mode, NMOS will be kept ON allowing the circuit to operate normally. In inactive mode NMOS will be turned OFF which supply high resistance path between the power supply and ground. The NMOS is kept ON/OFF by means of controlling input Sin.

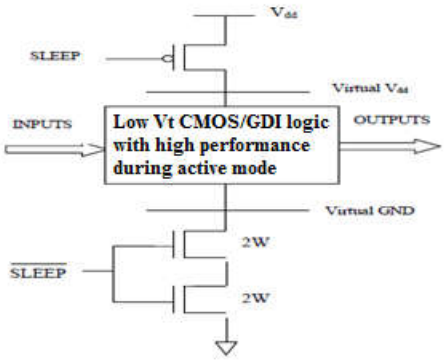


Fig.7. Logic diagram of proposed method 1

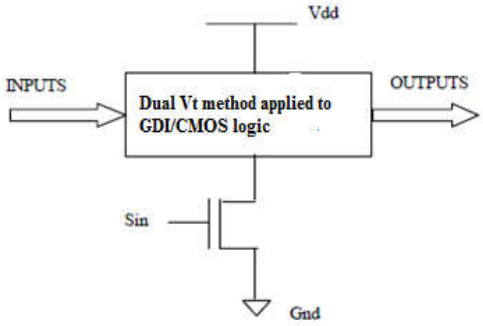


Fig.8. Logic diagram of proposed method 2

### C) Proposed method 3

In the proposed design, a PMOS transistor is kept above the developed design logic which in-turn cut-off the power supply to the logic block when it is in inactive mode.

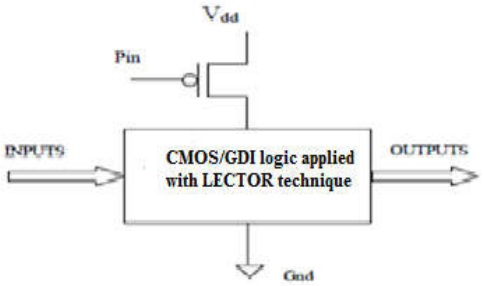


Fig.9. Logic diagram of proposed method 3

### D) Proposed method 4

Drain gating technique was used previously. Now this technique was improved and is known as drain footer with power header (DFPH). Here a PMOS sleep transistor is placed above the PUN and NMOS sleep transistor is placed above the PDN and the figure is shown in leakage reduction methods using drain gating.

Main steps in this project is,

1. Implement 2:1 multiplexer, 4:1 multiplexer, half adder, full adder and basic gates using static logic.
   Find active and standby power, current, delay and transistor count for all circuits.
2. Then using GDI logic implement 2:1 multiplexer, 4:1 multiplexer, half adder, full adder and basic gates.
   Find active and standby power, current, delay and transistor count for all circuits.

3. Implement all leakage current reduction methods using a simple static/GDI inverter by reducing the supply voltage (Vdd) and find best 5 leakage current reduction methods.
4. Implement all these circuits of static and GDI logic with 5 best leakage current reduction methods.
5. Implement all these circuits of static and GDI logic again with proposed reduction methods. Find active and standby power, current, delay and transistor count of all methods.
6. Implement 4bit and 8bit ALU using the best power reduction method.

The multiplexer stages is capable of selecting suitable inputs based on the condition of the select signals, and gives it to the full adder which then compute the results. The multiplexer at the output stage selects the appropriate output and route it to output stage of the design. Table 3 shows the truth table for the operations performed according to the status of the select signal to by the ALU (22). Finally, the operation will be performed and the inputs given based on the three select signal of multiplexer and outputs are determined according to the three select signals incorporated in the design. Figure 8 shows multiplexer logic at input port and Figure 9 shows multiplexer logic at output the stage.

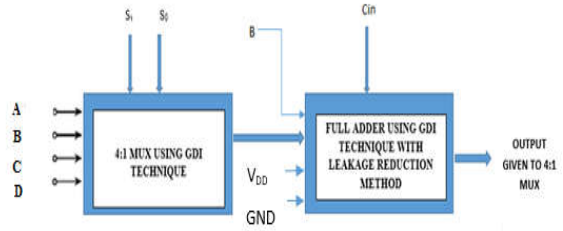


**Fig.10. Block diagram of multiplexer logic at the input**

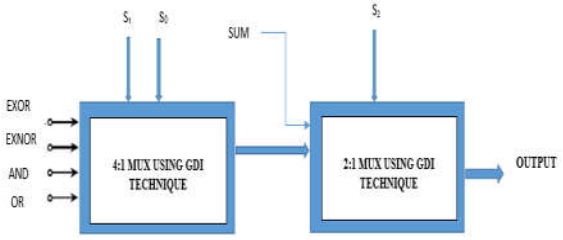


**Fig.11. Block diagram of multiplexer logic at the output**

The ALU schematic is designed using schematic editor of Tanner EDA. The 4-bit ALU consists of two 4-bit inputs, three selecting lines from multiplexer stage and four output bits. Also there were carry out and carry signals from the full adder stages. This paper gives a new approach using an abstract idea of Gate Diffusion Input Technique to design an arithmetic and logic unit. Also, using GDI technique along with leakage reduction methods ALU has implemented. In an ALU, the most important thing is to achieve appropriate input selection of multiplexer in order to perform a particular operation and for obtaining output accordingly. An ALU is a digital circuit used for performing many functions like arithmetic and logic operations. ALU is considered as the basic building block of the Central Processing Unit (CPU) of a computer system. Arithmetic operations like addition, subtraction, increment, decrement, transfer, etc. and logic functions like AND, OR, XOR, XNOR etc. are performed in ALU. This deals with the design of an 8- bit ALU which performs the foresaid functions.

**Table 5. ALU Operations**

| $S_2$ | $S_1$ | $S_0$ | Operations |
|---|---|---|---|
| 0 | 0 | 0 | And |
| 0 | 0 | 1 | EXOR |
| 0 | 1 | 0 | EXNOR |
| 0 | 1 | 1 | Or |
| 1 | 0 | 0 | Addition |
| 1 | 0 | 1 | Subtraction |
| 1 | 1 | 0 | Increment |
| 1 | 1 | 1 | Decrement |

The 8 bit ALU consists of sixteen 4x1 multiplexers, eight 2x1 multiplexers and eight full adders. The functions are performed on the basis of select line combinations. When S2 = 0, arithmetic functions are performed. Logic functions will be performed when S2 = 1. Increment operation is performed by the addition of "1" to the addend and decrement operation is performed by the complement addition. For subtraction Two's complement method is used in which complement of B is used. The functions obtained from the full adder are Addition, Subtraction, Increment, Decrement and Transfer. The functions AND, XOR and XNOR are obtained from the half adder and an OR gate is used to get the OR function.

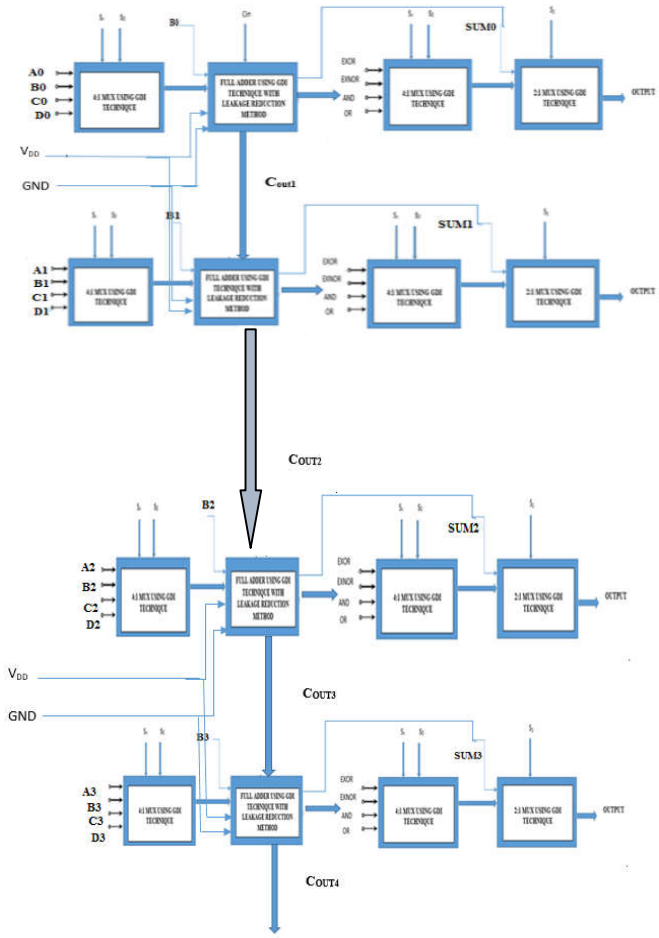


**Fig.12. Block Diagram of 4-bit Arithmetic and Logic Unit**

## RESULTS

Supply voltage reduction was done with the help of static inverter in 95nm technology with width, W=150u (PMOS) and 75u (NMOS). Static inverter will invert the input and gives inverted output. When input is 1 output will be 0 and vice versa. Leakage power is found by taking the input pulse's $V_{high}$ and $V_{low}$ at 0 volt. In order to work all circuits properly $V_{DD}$ is taken as 1.8 volt. But delay increases with reduction in $V_{DD}$. Here almost 20 leakage reduction methods were identified then simulation was done using static inverter in 95nm technology and width W is take as W=150u and 75u for NMOS and PMOS respectively. Leakage power is found by taking the input pulse's $V_{high}$ and $V_{low}$ at 0 volt. During this time PMOS sleep transistor will be ON and NMOS sleep transistor will be OFF.

### A) Simulation using circuits of Static & GDI logics

Leakage power is found by taking the input pulse's $V_{high}$ and $V_{low}$ at 0 volt. During this time PMOS sleep transistor will be ON and NMOS sleep transistor will be OFF. Table 8 and 9 shows the simulation results.

**Table 6. Leakage Power Reduction methods**

| Techniques | $V_{DD}$ in volt | Delay (sec) | Power consumption (watt) | Current (μA) | Leakage power (watt) | Transistor count |
|---|---|---|---|---|---|---|
| Sleep transistor | 5 | 2.5831e-011 | 2.493062e-003 | 405 | 325e-012 | 4 |
| | 1.8 | 2.9310e-011 | 3.2623985e-004 | 150 | 149.4e-012 | |
| Sleepy stack | 5 | 2.0439e-011 | 4.194749e-003 | 425 | 325e-012 | 6 |
| | 1.8 | 2.0502e-011 | 3.231260e-004 | 155 | 99e-012 | |
| Sleepy keeper | 5 | 1.3020e-010 | 2.475349e-003 | 449.5 | 410e-012 | 6 |
| | 1.8 | 1.4743e-010 | 3.248473e-004 | 160 | 131.4e-012 | |
| Forced stacking | 5 | 1.7978e-011 | 2.496666e-003 | 345 | 540e-012 | 3 |
| | 1.8 | 1.8063e-011 | 3.236710e-004 | 124 | 185.4e-012 | |
| Normal stacking | 5 | 3.2069e-011 | 1.360625e-003 | 460 | 200e-012 | 4 |
| | 1.8 | 4.7742e-011 | 4.753127e-004 | 170 | 81e-012 | |
| Dual sleep | 5 | 2.5813e-011 | 7.704740e-004 | 405 | 690e-012 | 6 |
| | 1.8 | 2.9227e-011 | 1.563368e-004 | 150 | 324e-012 | |
| Dual stack | 5 | 3.6167e-012 | 8.551110e-001 | 252 | 2070e-012 | 8 |
| | 1.8 | 5.2506e-008 | 9.749308e-002 | 49 | 2070e-012 | |
| Triple stack | 5 | 1.8078e-011 | 6.566464e-004 | 345 | 1.7e-009 | 9 |
| | 1.8 | 1.7609e-011 | 3.241254e-004 | 124 | 594e-012 | |
| Sleepy pass gate | 5 | 7.2021e-011 | 2.498031e-003 | 375 | 0.7e-009 | 4 |
| | 1.8 | 5.0362e-011 | 3.233636e-004 | 140 | 261e-012 | |
| LECTOR | 5 | 2.7469e-011 | 2.495894e-003 | 290 | 0.75e-009 | 4 |
| | 1.8 | 2.5090e-011 | 3.242068e-004 | 90 | 234.36e-012 | |
| Zigzag | 5 | 5.8394e-011 | 2.586288e-001 | 300 | 4.3e-007 | 6 |
| | 1.8 | 5.6853e-011 | 3.151375e-002 | 160 | 9.0e-010 | |
| Drain gating | 5 | 4.3778e-011 | 2.495626e-003 | 365 | 77.5e-012 | 4 |
| | 1.8 | 4.9767e-011 | 3.243899e-004 | 140 | 21.24e-012 | |
| DHPF | 5 | 3.6771e-011 | 2.492808e-003 | 365 | 77.5e-012 | 4 |
| | 1.8 | 4.2232e-011 | 3.163417e-004 | 140 | 21.24e-012 | |
| VCLEARIT | 5 | 1.1319e-011 | 2.499241e-003 | 365 | 27.60e-009 | 5 |
| | 1.8 | 1.3444e-011 | 3.245676e-004 | 134 | 829.8e-012 | |
| GALEOR | 5 | 1.1735e-011 | 2.431195e-003 | 265 | 5.5e-012 | 4 |
| | 1.8 | 1.3677e-011 | 2.785718e-004 | 98 | 1.8036e-012 | |
| MTCMOS | 5 | 2.9251e-011 | 2.416750e-003 | 415 | 0.025e-006 | 4 |
| | 1.8 | 2.4687e-011 | 3.229683e-004 | 158 | 0.486e-009 | |
| DTCMOS | 5 | 2.3177e-011 | 2.404940e-003 | 420 | 2.55e-009 | 4 |
| | 1.8 | 2.2535e-011 | 3.414535e-004 | 150 | 0.414e-009 | |
| SCCMOS | 5 | 1.3934e-011 | 2.495060e-003 | 410 | 0.925e-009 | 4 |
| | 1.8 | 2.9303e-011 | 3.242589e-004 | 150 | 324e-012 | |
| Zigzag with keeper | 5 | 6.6456e-011 | 2.586293e-001 | 300 | 9.5e-009 | 8 |
| | 1.8 | 6.3543e-011 | 3.151326e-002 | 160 | 9.54e-010 | |
| Dual threshold | 5 | 1.8396e-010 | 2.490304e-003 | 480 | 0.85e-009 | 4 |
| stack transistor | 1.8 | 9.9333e-011 | 2.163064e-004 | 175 | 288e-012 | |
| Variable body | 5 | 3.0485e-011 | 2.487613e-003 | 375 | 150e-012 | 6 |
| biasing | 1.8 | 2.8286e-011 | 3.227136e-004 | 128 | 54e-012 | |
| Leakage feedback | 5 | 3.7124e-011 | 4.228019e-001 | 415 | 0.85e-009 | 8 |
| | 1.8 | 6.4003e-011 | 5.171465e-002 | 155 | 295.2e-012 | |

**Table 7. Supply Voltage reduction table**

| | $V_{DD}$(volt) | Delay(ns) | Power consumption (watt) | Current (μA) |
|---|---|---|---|---|
| Static inverter With 2 Transistors | 5 | 1.7300e-011 | 1.386703e-003 | 405 |
| | 2.5 | 1.4936e-011 | 1.190177e-003 | 205 |
| | 1.8 | 1.5759e-011 | 5.135588e-004 | 145 |
| | 1 | 2.0661e-011 | 1.58987e-004 | 70 |

**Table 8. Simulation using circuits of static logic**

| CIRCUIT | $V_{DD}$ (V) | DELAY (sec) | CURRENT(μA) | POWER CONSUMPTION(watt) | LEAKAGE POWER (watt) | TRANSISTOR COUNT |
|---|---|---|---|---|---|---|
| INVERT-ER | 1.8 | 1.5759e-011 | 145 | 5.135588e-004 | 270e-012 | 2 |
| AND GATE | 1.8 | 4.1364e-011 | 126 | 5.130234e-002 | 2.88e-010 | 6 |
| OR GATE | 1.8 | 4.3181e-011 | 145 | 5.130306e-002 | 1.44e-010 | 6 |
| XOR GATE | 1.8 | 4.8594e-008 | 121 | 9.404702e-002 | 3.06e-010 | 12 |
| XNOR GATE | 1.8 | 2.0003e-007 | 121 | 5.162693e-002 | 3.08e-010 | 12 |
| HALF ADDER | 1.8 | 4.0929e-011 | 126 | 9.404699e-002 | 3.42e-010 | 18 |
| FULL ADDER | 1.8 | 4.0637e-011 | 145 | 1.026092e-001 | 4.57e-010 | 28 |
| 2:1 MUX | 1.8 | 4.6167e-011 | 135 | 5.130394e-002 | 1.62e-010 | 12 |
| 4:1 MUX | 1.8 | 5.8523e-011 | 145 | 5.130463e-002 | 4.98e-010 | 30 |

**Table 9. Simulation using circuits of GDI logic**

| CIRCUITS | DELAY (sec) | CURRENT (μA) | POWER CONSUMPTION (watt) | LEAKAGE POWER (watt) | TRANSISTOR COUNT |
|---|---|---|---|---|---|
| INVERTER | 1.5759e-011 | 145 | 5.135588e-004 | 270e-012 | 2 |
| AND GATE | 1.3171e-010 | 131 | 2.738302e-022 | 0 | 2 |
| OR GATE | 5.2007e-011 | 175 | 1.649100e-007 | 164.7e-009 | 2 |
| XOR GATE | 1.6105e-010 | 138 | 1.251621e-006 | 0.0252e-009 | 4 |
| XNOR GATE | 2.0003e-007 | 67 | 3.160300e-004 | 468e-009 | 6 |
| HALF ADDER | 8.5339e-011 | 126 | 1.260771e-006 | 0.0288e-009 | 6 |
| FULL ADDER | 5.6892e-010 | 130 | 4.826583e-007 | 6.702e-009 | 10 |
| 2:1 MUX | -3.9186e-012 | 175 | 6.110182e-022 | 0 | 2 |
| 4:1 MUX | -3.3362e-011 | 165 | 7.570091e-023 | 0 | 6 |

**Table 10. Simulation of 10T GDI full adder with leakage reduction methods**

| 10T GDI FULL ADDER | DELAY (sec) | CURRENT (μA) | POWER CONSUMPTION (watt) | LEAKAGE POWER (watt) | TRANSISTOR COUNT |
|---|---|---|---|---|---|
| LECTOR | 5.6043e-010 | 128 | 2.211359e-006 | 3.42e-007 | 14 |
| GALEOR | 9.6425e-011 | 90 | 4.991937e-006 | 5.94e-012 | 14 |
| DRAIN GATING | 5.7361e-010 | 127 | 2.433524e-006 | 2.3364e-007 | 14 |
| MTCMOS | 7.0956e-010 | 129.5 | 3.474933e-007 | 0.019908e-009 | 14 |
| DTCMOS | 6.1272e-010 | 130 | 2.476372e-007 | 0.0792e-009 | 14 |

**Table 11. Simulation of 10T GDI full adder with proposed leakage reduction methods**

| 10T GDI FULL ADDER | DELAY (sec) | CURRENT (μA) | POWER CONSUMPTION (watt) | LEAKAGE POWER (watt) | TRANSISTORC OUNT |
|---|---|---|---|---|---|
| LECTOR | 6.0985e-010 | 120 | 2.213183e-006 | 7.4472e-008 | 16 |
| DRAIN GATING USING DFPH | 6.4222e-010 | 128 | 2.433570e-006 | 1.188e-009 | 14 |
| MTCMOS | 6.2396e-010 | 129.5 | 4.4940626e-007 | 0.019836e-009 | 16 |
| DTCMOS | 5.5505e-010 | 130 | 3.707477e-007 | 0.0161874e-009 | 16 |

**Table 12. Power comparison table**

| Logic style | Total power (μWatts) | | Transistor count | |
|---|---|---|---|---|
| | 4bit ALU | 8bit ALU | 4bit ALU | 8bit ALU |
| ALU using conventional logic | 1.0260896 Watts | 2.0521792 Watts | 400 | 800 |
| ALU using GDI logic | 1.93368288 | 3.86736576 | 96 | 192 |
| ALU using GDI logic with MTCMOS method | 1.39302288 | 2.78604576 | 112 | 224 |
| ALU using GDI logic with DTCMOS method | 0.99359848 | 1.98719696 | 112 | 224 |
| ALU using GDI logic with Drain gating method | 9.73714568 | 19.47429136 | 112 | 224 |
| ALU using GDI logic with GALEOR method | 19.97079768 | 39.94159536 | 112 | 224 |
| ALU using GDI logic with LECTOR method | 8.84848568 | 17.69697136 | 112 | 224 |
| ALU using GDI logic with Proposed MTCMOS method | 1.97930008 | 3.95860016 | 120 | 240 |
| ALU using GDI logic with Proposed DTCMOS method | 1.48604048 | 2.97208096 | 120 | 240 |
| ALU using GDI logic with Proposed DFPH method | 9.73732968 | 19.47465936 | 112 | 224 |
| ALU using GDI logic with Proposed LECTOR method | 8.85578168 | 17.71156336 | 120 | 240 |

### B) Simulation using Leakage Reduction Methods in 10T GDI Full Adder

Simulation was done in 95nm technology and width W is take as W=150u and 75u for NMOS and PMOS respectively. Leakage power is found by taking the input pulse's $V_{high}$ and $V_{low}$ at 0 volt. During this time PMOS sleep transistor will be ON and NMOS sleep transistor will be OFF. In GDI logic full adder was implemented using 10 transistors. Simulation results are shown in Table 10.

### C) Simulation using Proposed Leakage Reduction Methods in 10T GDI Full Adder

10T GDI full adder was implemented using four different proposed methods as mentioned above. Simulation results can be seen in Table 11.

### D) ALU Simulation

Arithmetic and logic unit of 4-bit and 8-bit was implemented using four 2:1 multiplexer, four full adders and eight 4:1 multiplexer and these components were constructed by both static logic and GDI logic. The 2:1 Mux have only one select line, $S_0$ and output=$AS_0$ + $BS_0$bar. Likewise 4:1 Mux have two select lines $S_1$ and $S_0$. Thus output=A $S_0$bar $S_1$bar+ B $S_0$bar $S_1$ + C $S_0$ $S_1$bar + D $S_1$ $S_0$. Also ALU was designed using proposed leakage reduction methods using these logic styles.

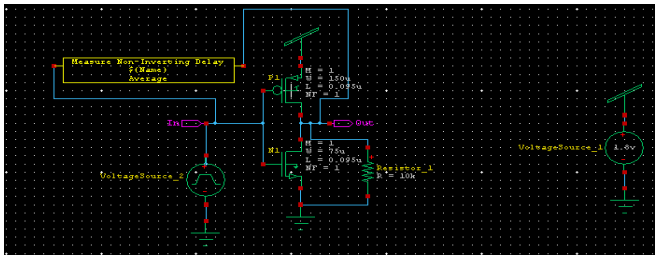


**Fig.13. Diagram of Static Inverter**

**Fig.14. Input and Output of Static Inverter at 1.8V**

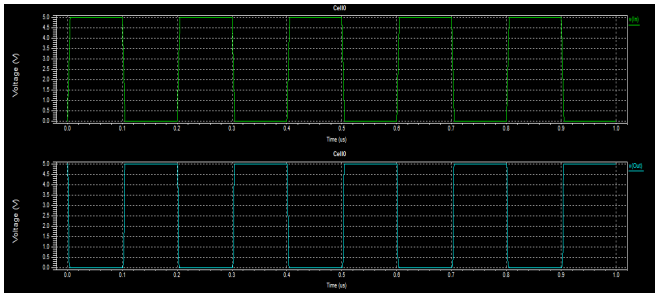

**Fig.15. Input and Output of Static Inverter at 5V**

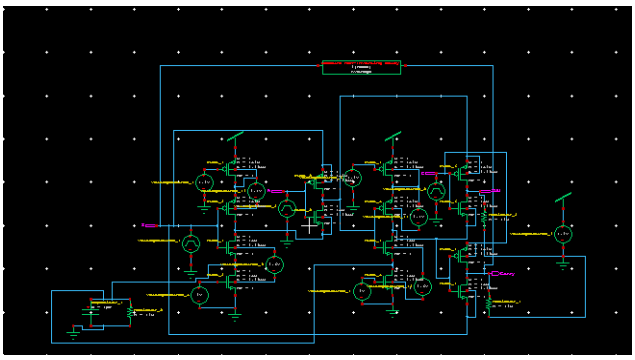

**Fig.16. Diagram of 10T GDI full adder using DTCMOS technique**

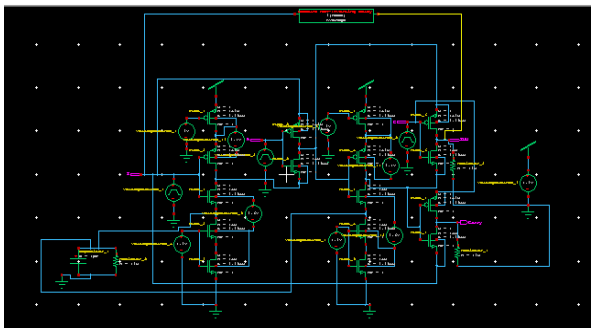

**Fig.17. Diagram of 10T GDI full adder using proposed DTCMOS technique**

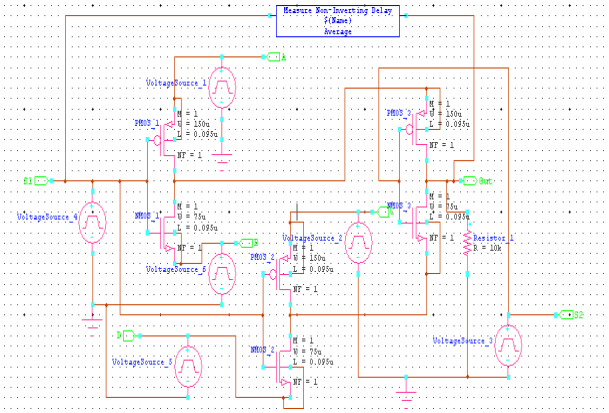

**Fig.18. Diagram of 4:1 MUX using GDI technique**

**Fig.19. Input of 4:1 GDI MUX**

**Fig.20. Output of 4:1 MUX using GDI technique**

The efficient method is using DTCMOS method in order to reduce the power consumption of a circuit. This method was introduced in GDI technique in order to minimize the area, transistor count and both static and dynamic power.

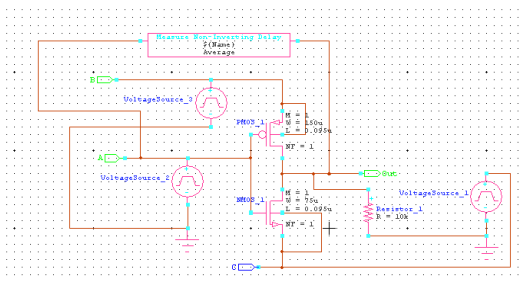

**Fig.21. Diagram of 2:1 MUX using GDI technique**

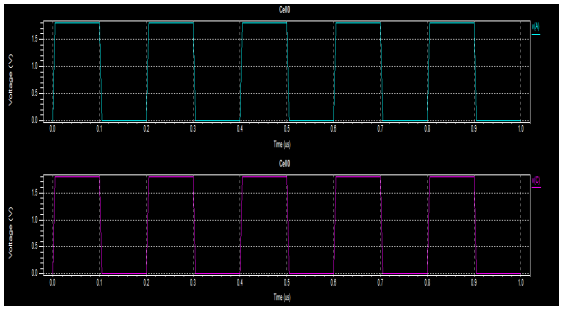

**Fig.22. Input of 2:1 GDI MUX**

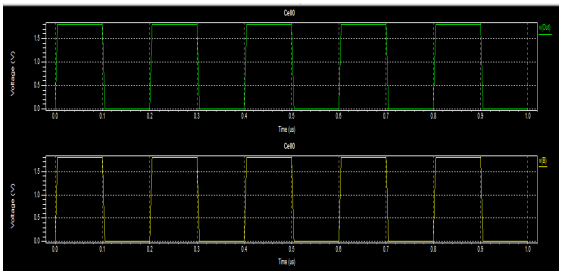

**Fig.23. Output of 2:1 GDI MUX**

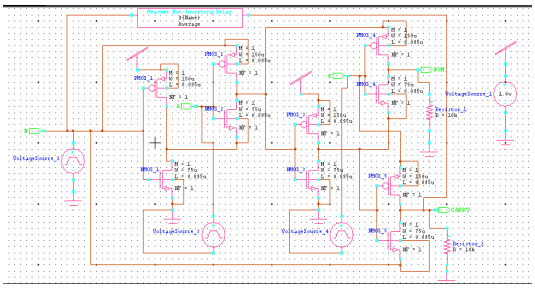

**Fig.24. Diagram of 10T full adder using GDI technique**

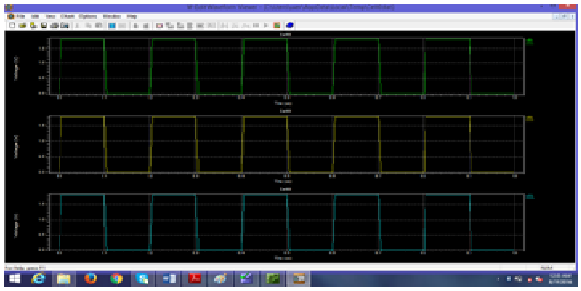

**Fig.25. Input of 10T GDI full adder**

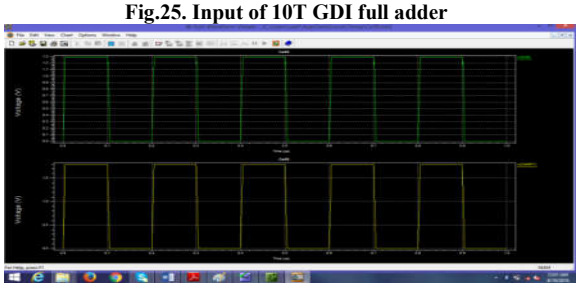

**Fig.26. Output (sum and carry) of 10T GDI full adder**

## CONCLUSION

Different topologies of multiplexer and full adder is studied and compared. The 2:1 multiplexer, 4:1 multiplexer and full adder with 10-transistors were designed using GDI cells and this is chosen for achieving low power consumption and minimum possible area. The dominant component of power consumption in CMOS circuits is dynamic power. Dynamic Power in a CMOS circuit is given by $P= C_L f V_{DD}^2$. The power supply is directly related to dynamic power. As the number of power supply to ground connections are reduced, the dynamic power consumption becomes very less. The leakage power is reduced by introducing leakage reduction techniques in both circuit styles. Power dissipation, propagation delay and the number of transistors of ALU were compared using Conventional CMOS and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques. Thus area and power consumption get reduced. The simulation is carried out in Tanner EDA 13.0 simulator using 0.095μm technologies.

## FUTURE ENHANCEMENTS

This paper mainly aims on,

- Reduction of standby power using leakage current techniques.
- Reduction of active power by supply voltage scaling.
- Thus reduces the total power consumption.
- Area reduction by using appropriate logics and by reducing transistor count.
- Proper transistor sizing

1. But one of the demerits is the increase in delay. So in future we will find to reduce the delay by reducing the supply voltage because here delay increases with scaling down of supply voltage ($V_{DD}$).
2. Now the techniques were applied to combinational circuits and can be extended to sequential circuits.
3. In this paper ALU was implemented using 10T full adder circuit with best leakage reduction method and in future this can be implemented using 9T, 8T, 7T and even using 6T full adder circuits. That is by using hybridizing PTL logic full adder circuits.

## ACKNOWLEGDEMENT

We thank the management of SCMS School of Engineering and Technology, HOD, teaching and non –teaching staffs of ECE department for their valuable support and guidance and also, for giving assistance in conducting simulations in the laboratory.

## REFERENCES

Abdollahi, A., Fallah, F., and Pedram, M. 2004. "Leakage Current Reduction in CMOS VLSI Circuits by Input Vector Control," IEEE Transactions on Very Large Scale Integration (VLSI) Systems 12, February, pp.140-154.

Anand N, George Joseph and Suwin Sam Oommen, "Performance Analysis and Implementation of Clock gating techniques for Low power applications", International Conference on Science, Engineering and Management Research (*ICSEMR* 2014) 978-1-4799-7613-3/14/$31.00 ©2014 IEEE.

ArchanaNagda *et al*. 2012. "Leakage Power Reduction Techniques: A New Approach", *International Journal of Engineering Research and Applications (IJERA)*, Vol. 2, Issue 2, Mar-Apr., pp.308-312.

Aswale P. S. and S. S. Chopade, 2013. "Comparative Study of Different Low Power Design Techniques for Reduction of Leakage Power in CMOS VLSI Circuits", International Journal of Computer Applications (0975 – 8887) Volume 70– No.11, May.

Dhananjay E, Upasani, Sandip B. Shrote, and Pallavi S. Deshpande, 2010. Standby Leakage Reduction in Nanoscale CMOS VLSI Circuits, *International Journal of Computer Applications, 7(5),* 1-4.

Divya R. and J.Muralidharan, 2013. "Leakage Power Reduction Through Hybrid Multi-Threshold CMOS Stack Technique In Power Gating Switch", *International Journal of Advanced Research in Computer Engineering & Technology (IJARCET),* Volume 2, Issue 4, April.

Jaffari J. and A**.** Afzali-Kusha, 2004. "New Dual-Threshold Voltage Assignment Technique for Low-Power Digital Circuits," 0-7803-8656-6/04/$20.00, pp.413-416 IEEE.

Jagadeesh, C., R. Nagendra and Neelimakoppala, 2013. "Design & Analysis of Different Types of Sleepy Methods for Future Technologies", *International Journal of Engineering Trends and Technology (IJETT),* - Volume4 Issue4- April.

James T. Kao and Anantha P. Chandrakasan, "Dual- Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 7, JULY 2000

Kaushal Kumar Nigam and Ashok Tiwari, 2012. "Zigzag Keeper: A New Approach For Low Power CMOS Circuit", *International Journal of Advanced Research in Computer and Communication Engineering,* Vol. 1, Issue 9, November.

Kawaguchi, H., Nose, K., and Sakurai, T. 2000. "A Super Cut-Off CMOS (SCCMOS) Scheme for 0.5-V Supply Voltage with Pico ampere Stand-By Current," *IEEE Journal of Solid State Circuits,* vol.35, n.10, October, pp.1498-1501.

Kim N. *et al*. 2002. "Drowsy Instruction Caches: Leakage Power Reduction Using Dynamic Voltage Scaling and Cache Sub-bank Prediction," *Proc. 35th Ann. Int'l Symp. Micro architecture* (MICRO-35), IEEE CS Press, pp. 219-230.

Malviya *et al*. 2013. "A new approach for Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS circuit for VLSI Applications", *International Journal of Advanced Research in Computer Science and Software Engineering,* 3(5), May, pp. 318-325.

Mutoh. S. *et al*. 1995. 1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS. *IEEE Journal of Solid-State Circuits*, 30, 847-854.

Park, J. C., and Mooney III, V. J. 2006. "Sleepy Stack Leakage Reduction," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 14, Nov 2006, pp.1250-1263.

PriyankaVerma and J. Selvakumar, "A Low Power Hybrid Clock Gating Technique for High Frequency Applications", 978-1-4799-7678-2/15/$31.00 ©2015 IEEE.

Pushpa Saini and Rajesh Mehra, 2012. Leakage Power Reduction in CMOS VLSI Circuits, *International Journal of Computer Applications*, *55(8),* 42-48.

Smita Singhal, Nidhi Gaur, Anu Mehra and Pradeep Kumar, 2015. "Analysis and Comparison of Leakage Power Reduction Techniques in CMOS circuits", 978-1-4799-5991-4/15/$31.00 ©2015 IEEE.

Srikanth Katruea and Dhireesha Kudithipudi, 2008. "GALEOR: leakage reduction for CMOS circuits", IEEE, Electronics circuits and systems, pp. 574-577, September.

Varsha Bendre and Dr. A. K. Kureshi, "An Overview of Various Leakage Power Reduction Techniques in Deep Submicron Technologies", 978-1-4799-6892-3/15 $31.00 © 2015 IEEE.

Vinny Wilson, "Analysis and Performance evaluation of 1-bit full adder using different Topologies", International Journal of Engineering Research & General Science (IJERGS), Vol.-5, Issue-1, Jan-Feb-2017.

Vivechana Dubey and Hari Mohan Rai, 2016. "GDI Technique based Low power and Area Proficient 4-bit Arithmetic Logic Unit", *International Journal of Engineering Research & Advanced Innovation (IJERAI)*, Vol.-1, Issue-2, June.

Wang, A., B.H. Calhoun, A.P. Chandrakasan, 2006. Sub-threshold Design for Ultra Low-power Systems, Springer.

*******