



RESEARCH ARTICLE

AN EFFICIENT ERROR DETECTION AND CORRECTION TECHNIQUE FOR MEMORIES
USING MLDD

^{*},¹Jinendra. D. Bhandekar and ²Navalgund, S. S.

¹P.G. Student, Department of ECE, SDM College of Engineering and Technology, Dharwad
²Assistant Professor, Department of ECE, SDM College of Engineering and Technology, Dharwad

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ABSTRACT

Memory is an important component of an embedded system. Memory testing is very complex. Large error rates are occurring because of technology scaling and also due to higher integration densities. Soft errors are considered as one of the problems with respect to the memories. This paper focuses on the design of an efficient system, that detects and corrects the error. Hence, the number of cycles required to detect and correct the error is also less. EG-LDPC codes, that is, Euclidean Geometry Low Density Parity Check codes are used here. Previous method like Majority Logic Decoding requires more number of cycles for detection and correction of error. But, this paper deals about Majority Logic Detector/Decoder (MLDD) technique wherein error detection and correction takes place in less number of cycles. Hence, the speed of operation can be increased, power consumption can be reduced and also area required for this technique is very less.

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INTRODUCTION

The memory is an important and universal component of an embedded system. Memories should always be protected from soft errors. In the digital communication, data received must always be same as data transmitted. The information stored in the memory gets changed due to many reasons. Some of the reasons are changes in the operating voltage, changes in the dimensions of the device, etc. But, whenever an error occurs, it must be quickly detected and corrected. There are many techniques that are used to detect and correct the errors. Both memories and nano-memories can be protected from soft errors using an efficient error detection and correction technique. This paper deals about an important error detection and correction method which can be applied for any type of memories. Hence, this paper deals about the error detection and correction technique for EG-LDPC codes. The decoding time for this method is very less. Maximum three cycles are required to detect the error using efficient MLDD. 'N' number of cycles are required for error correction.

Literature Survey

There are many methods for error detection and correction. TMR i.e. Triple Modular Redundancy and ECC i.e. Error Correction Codes are some of the error detection methods. Majority Logic Decoding is another technique that is used for error correction. ML Decoding method has many advantages. ML Decoding is simple and it has less complexity. Majority Logic Decoder is shown in Fig. 1. For this, EG-LDPC codes are used. (15,7,5) Euclidean Geometry Low Density Parity Check codes are used for error correction. This corrector has four ex-or gates, with codewords as input. Later, the outputs from the ex-or gates are sent to the ML circuit. Finally, the output of ML circuit is ex-ored with C14 bit to get new C0 value. Hence, this process continues for 'N' number of cycles. 'N' is the length of the codeword. The length of the codeword depends on the length of the message bits. Here, there are seven message bits and fifteen codewords. The flowchart for this method is explained in Fig. 2. In the ML circuit, the number of '0' and number of '1' are counted. If number of 1 is greater than number of 0, then the corresponding bit is changed using ex-or gate. Otherwise, the corresponding bit is not changed. If errors are present in the codeword, then corrected codeword is obtained after 'N' cycles using above method.

*Corresponding author: Jinendra. D. Bhandekar
P.G. Student, Department of ECE, SDM College of Engineering and Technology, Dharwad

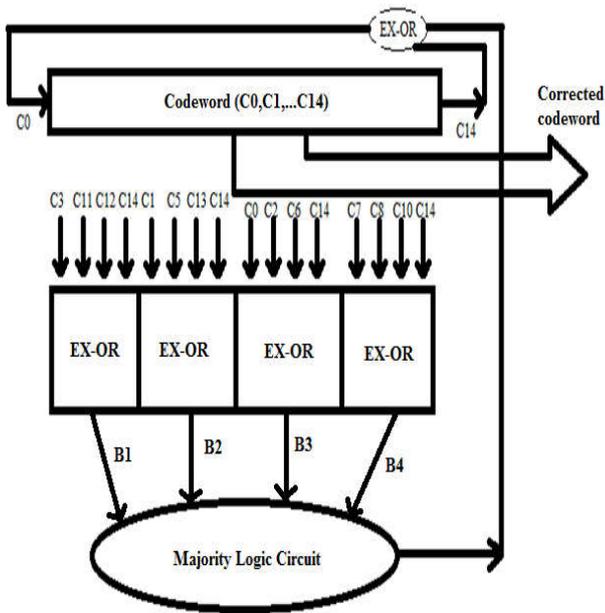


Fig. 1. ML Decoder for error correction (Dandem Sudhakar and Indrani, 2015)

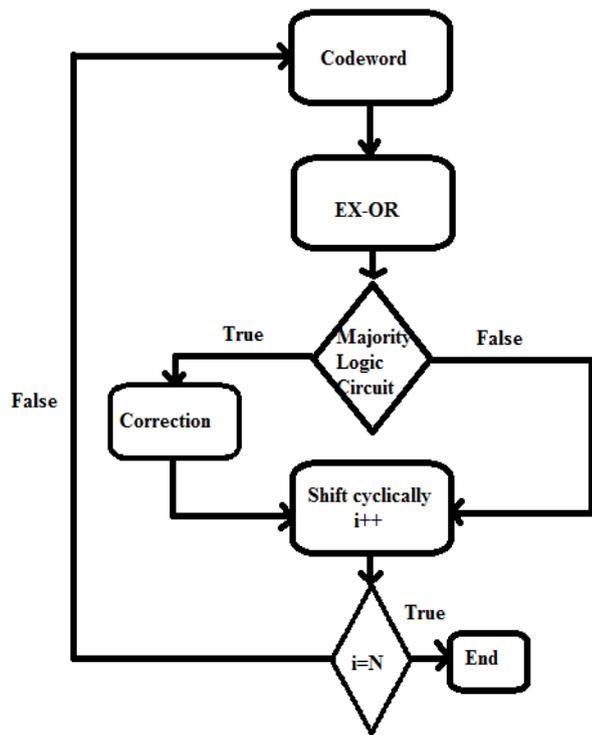


Fig. 2. Flowchart (Dandem Sudhakar and Indrani, 2015)

But, if no errors are present in the codeword, then also ‘N’ iterations are required to determine that no error is present in the codeword. This is the major disadvantage of this method. Therefore, an efficient error detection and correction method will be explained in this paper.

MATERIALS AND METHODS

This section deals about the efficient error detection and correction methodology. The efficient ML Detector/Decoder is used for detecting and correcting the error. EG-LDPC codes are used for this method. In this section, the encoding method, the efficient decoding method and the control logic are explained. For the encoding and decoding methods, (15,7,5)

EG-LDPC codes are used. Using this method, the errors present in the codeword can be detected in three cycles only. If there are no errors in the codeword, then also it requires three cycles for detection. But, the number of cycles for error correction depends on the length of the codeword.



Fig. 3. Memory and the efficient MLDD

The memory system is shown in Fig. 3. The message bits are initially encoded. Later they are stored in the memory. The information bits that are stored in the memory can get changed because of various reasons like changes in the operating voltage, integration densities, etc. To detect and correct these errors in the codeword, efficient MLDD is used. It can detect the errors in only three cycles.

Encoder Circuit

The generator matrix is shown in Fig. 4. It is an important matrix because the encoder circuit depends on the generator matrix. (15,7,5) Euclidean Geometry Low Density Parity Check codes are used for the encoding method. Generator matrix consists of unit matrix and parity matrix.

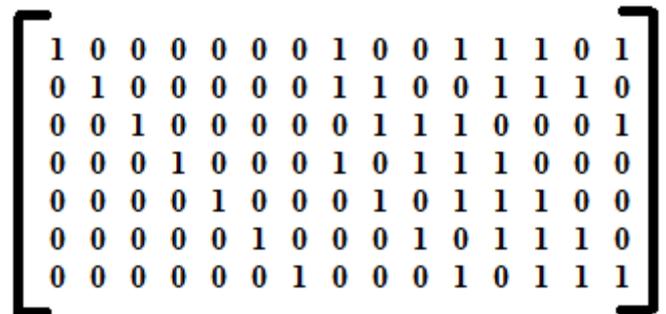


Fig. 4. Generator matrix [9]

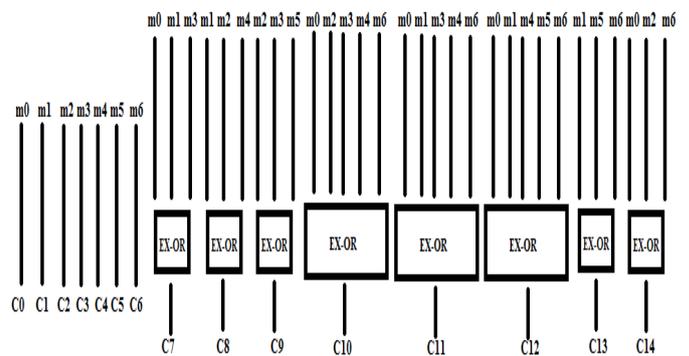


Fig. 5. Encoder circuit

The encoder circuit is shown in Fig. 5. Seven message bits are used and fifteen codewords are obtained from the encoder circuit. From the encoder circuit, codewords C0 to C14 are obtained. The first 7-bits of the codeword is same as that of message bit. The remaining codewords from C7 to C14 are obtained by the ex-or gates. Hence, there are seven information bits and eight parity bits.

Flowchart of efficient MLDD

The flowchart of efficient MLDD is shown in Fig. 6. Initially the codewords are given as input. Later, the corresponding bits of the codeword is ex-ored. Then, the output of the ex-or gates are sent to the control logic as well as the majority logic circuit. Control logic detects the errors in the codeword. If there are no errors in the codeword, the decoding process is stopped after three cycles. But, if there are errors in the codeword, then the correction of the codeword takes place. Fifteen cycles are required for error correction.

As shown in Fig. 6, the output of the 2nd OR gate is important. Because if the output is 1, it means there is error in the codeword. If the output is 0, it means there is no error in the codeword. The error if present in the codeword has to be corrected. In the ML circuit, if number of 1 is greater than number of 0, then the bit is corrected. Then the codeword can be shifted. Therefore, as shown in the flowchart, the error correction requires ‘N’ cycles. Error detection and correction can be made for any length of codeword using this efficient MLDD method. Hence, this method can be used for any type of memory.

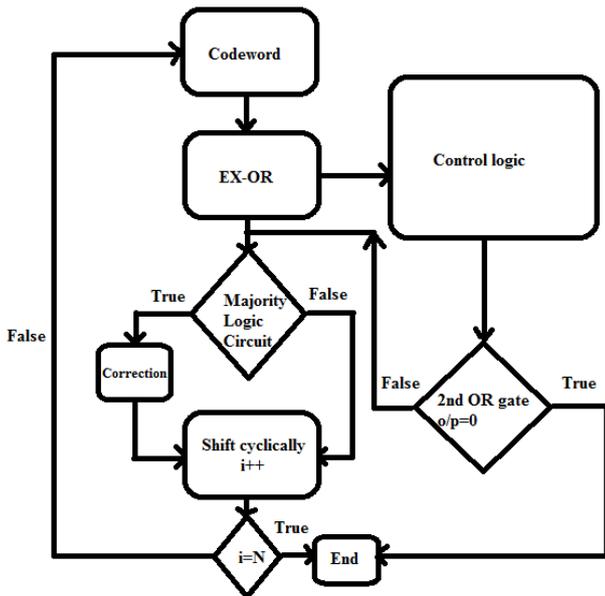


Fig. 6. Flowchart

Decoder Circuit

Efficient ML Detector/Decoder is used for error detection and correction. Fig. 7 depicts the efficient ML Detector/Decoder. The output of encoder circuit, that is 15-bit codewords are given as input to this efficient ML Detector/Decoder. Later, those codewords are sent to the ex-or gates as shown in Fig. 7. Here, 4-input ex-or gates are used. The output from the ex-or gates are sent to both ML circuit and control logic. Control logic is shown in Fig. 8. Control logic detects error in 3 cycles. If errors are present in the codeword, after 15 cycles the corrected codeword is obtained. B1, B2, B3, B4 are the outputs from the ex-or gates. C14th bit of the codeword is ex-ored with output of the ML circuit. The output of ML circuit depends on the values of B1, B2, B3 and B4. If B1, B2, B3 and B4 are 0, then output of ML circuit is 0. If any value of B1 to B4 is 1, then the output of ML circuit is 1.

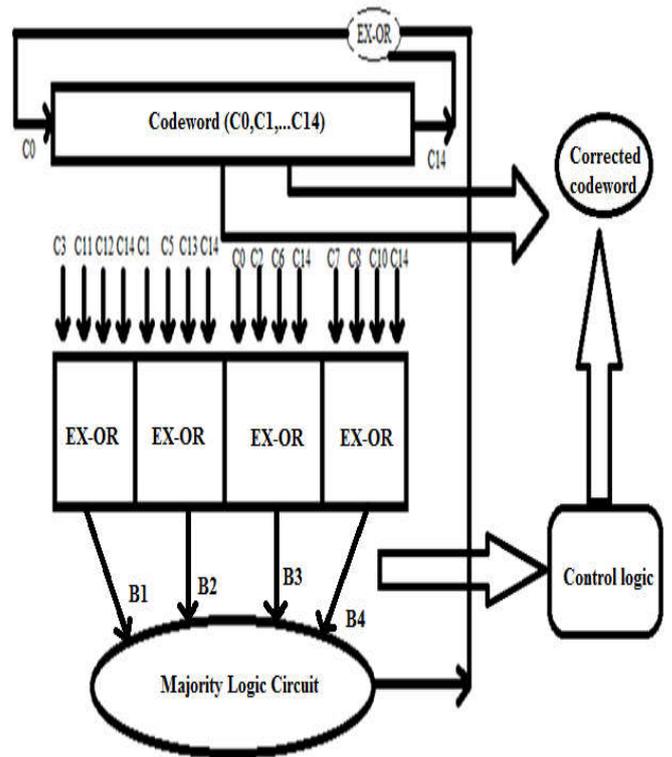


Fig. 7. Decoder circuit

C14 bit and ML circuit output are ex-ored to get new value of C0. The new C0 value is placed in its position, after shifting the previous codeword. Fig. 8 depicts the control logic. Control logic is required for error detection. The output from the 4-input ex-or gates are sent to the control logic. In the 1st cycle, the output from 1st OR gate is stored in the first register. In the 2nd cycle, the output from 1st OR gate is stored in the first register by shifting its previous value to the second register. In the 3rd cycle, the output from 1st OR gate is directly sent as input to the 2nd OR gate. The other two inputs to the 2nd OR gate are the values stored in the registers. If the output of 2nd OR gate is 0, it means there is no error in the codeword. But, if the output of the 2nd OR gate is 1, it means there is error in the codeword. The error present in the codeword has to be corrected.

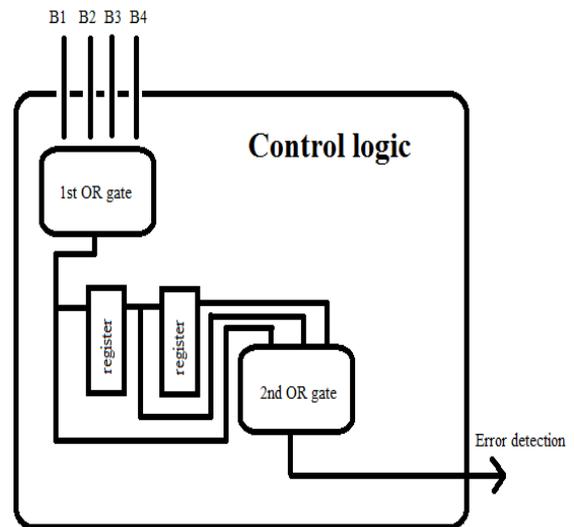


Fig. 8. Control logic of efficient MLDD

In the control logic, the 1st OR gate is having four inputs and the 2nd OR gate is having three inputs. Each register stores single bit value.

RESULTS AND ANALYSIS

This section deals about the results and analysis. The software used to design the efficient error detector and corrector is Xilinx ISE 14.3. The code is written in Verilog HDL. The length of the message bits is 7 and length of the codeword is 15.

Output of the encoder

Encoder circuit is an important circuit because, the message bits are encoded. Here, message bits of length 7-bits are used for encoding. The output of the encoder circuit is of length 15-bits. The RTL schematic for encoder circuit is shown in Fig. 9. Here, d0 to d6 are the seven inputs. C0 to C14 are the fifteen outputs. The simulation results for the encoder is shown in Fig. 10. For the various inputs, the outputs are obtained. Here, d0 to d6 are the message bits and they are of 7-bits. These message bits are encoded to get the codewords. The codewords has two parts. That is, it consists of information bits and parity bits. Here, there are 7 information bits and 8 parity bits in the codeword. The information bits of the codeword is same as the message bits. But, the corresponding information bits are XORed to get the parity bits. In the simulation result, the corresponding codeword is obtained for the input message bits.

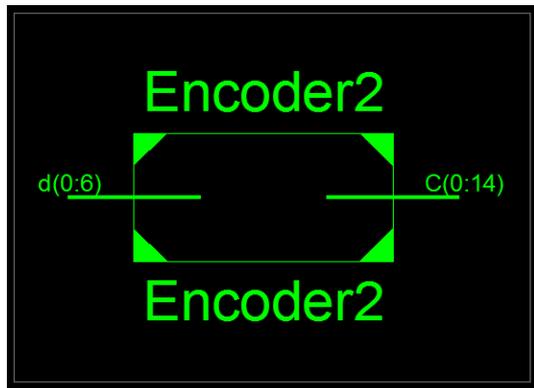


Fig. 9. RTL schematic of the encoder

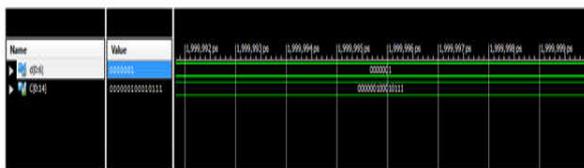


Fig. 10. Simulation results of the encoder

Output of the decoder

Decoder detects and corrects the error present in the codeword. The RTL schematic of the efficient MLDD is shown in the Fig. 11. The codeword is given as the input to the efficient MLDD. This efficient MLDD has the control logic, that detects the error only in 3 cycles. If errors are present in the codeword, then 15 cycles are required to correct the codeword. The simulation results of the efficient MLDD is shown in the Fig. 12. Here, the codeword obtained from the encoder is given as

the input to the efficient MLDD. Hence, there is no error in the codeword. The efficient MLDD has many advantages compared to previous method like ML Decoding. The decoding time of the efficient MLDD is very less. Also, it occupies lesser area. The speed of operation of the efficient MLDD is high. Therefore, efficient MLDD can be used for all types of memories and nano-memories.

Table 1. Comparison between efficient majority logic detector/decoder and ml decoding techniques

Technique	Total no. of cycles	
	Detection of error	Correction of error
Efficient Majority Logic Detector/Decoder	3	N
ML Decoding	N	N

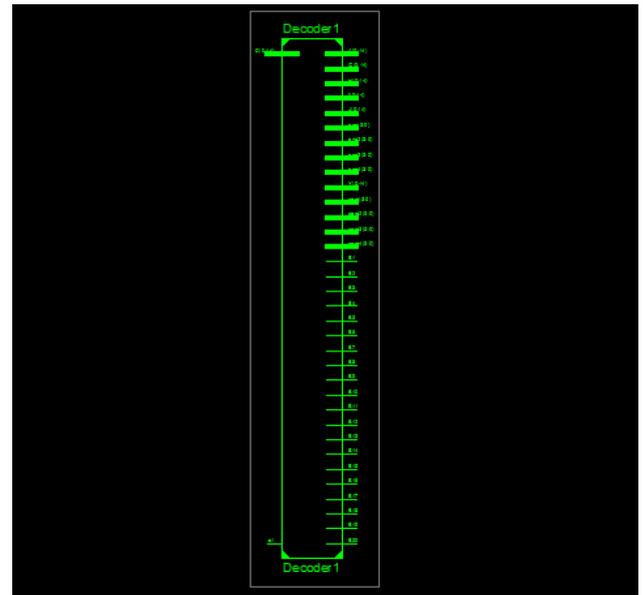


Fig. 11. RTL schematic of the decoder



Fig. 12. Simulation results of the decoder

Fig. 13 depicts the simulation results of the decoder. Here, the codeword with error is given as the input to the efficient MLDD. The error is detected and after 15 cycles the codeword is corrected. The comparison between the efficient MLDD and the previous MLD technique is shown in Table I. Efficient MLDD requires less decoding time.

Name	Value	[1,995,952]ps	[1,995,953]ps	[1,995,954]ps	[1,995,955]ps	[1,995,956]ps	[1,995,957]ps	[1,995,958]ps
C0[14]	00001100010111				00001100010111			
A0[14]	00001100010111				00001100010111			
S	0							
C9[14]	00000100010111				00000100010111			
F0[14]	11000111000101				11000111000101			
F1[14]	00000100010111				00000100010111			
F2[14]	00000100010111				00000100010111			
F3[14]	00000100010111				00000100010111			
F4[14]	00000100010111				00000100010111			
F5[14]	0001				0001			
F6[14]	0001				0001			
F7[14]	0001				0001			
F8[14]	0001				0001			
F9[14]	0011				0011			
F10[14]	0011				0011			
F11[14]	0011				0011			
F12[14]	0011				0011			
F13[14]	0011				0011			
F14[14]	0000				0000			
F15[14]	0							
F16[14]	1							
F17[14]	0							
F18[14]	0							
F19[14]	1							
F20[14]	0							
F21[14]	0							
F22[14]	0							
F23[14]	0							
F24[14]	0							
F25[14]	0							
F26[14]	0							
F27[14]	0							
F28[14]	0							
F29[14]	0							
F30[14]	0							
F31[14]	0							
F32[14]	0							
F33[14]	0							
F34[14]	0							
F35[14]	0							
F36[14]	0							
F37[14]	0							
F38[14]	0							
F39[14]	0							
F40[14]	0							
F41[14]	0							
F42[14]	0							
F43[14]	0							
F44[14]	0							
F45[14]	0							
F46[14]	0							
F47[14]	0							
F48[14]	0							
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F62[14]	0							
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F67[14]	0							
F68[14]	0							
F69[14]	0							
F70[14]	0							
F71[14]	0							
F72[14]	0							
F73[14]	0							
F74[14]	0							
F75[14]	0							
F76[14]	0							
F77[14]	0							
F78[14]	0							
F79[14]	0							
F80[14]	0							
F81[14]	0							
F82[14]	0							
F83[14]	0							
F84[14]	0							
F85[14]	0							
F86[14]	0							
F87[14]	0							
F88[14]	0							
F89[14]	0							
F90[14]	0							
F91[14]	0							
F92[14]	0							
F93[14]	0							
F94[14]	0							
F95[14]	0							
F96[14]	0							
F97[14]	0							
F98[14]	0							
F99[14]	0							

Fig. 13. Simulation results of the decoder

Conclusion

The design of an efficient Majority Logic Detector/Decoder is explained in this paper. This system can detect and correct the errors present in the codeword in less decoding time. This system can be used for memory applications. (15, 7, 5) EG-LDPC codes are used and detection of errors requires only 3 cycles for any length of the codeword. The control logic is an important component of the efficient MLDD. The efficient MLDD has high speed of operation compared to ML Decoding method. The number of components in the efficient MLDD are less and the overall area required for this system is very less. There are many disadvantages of the ML Decoding method. Therefore, efficient Majority Logic Detector/Decoder can be used.

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